datasheet

PRELIMINARY SPECIFICATION

1/3.06" color CMOS 13 megapixel (4208 x 3120) image sensor
with PureCel®Plus technology

OV13B10

color CMOS 13 megapixel (4208 x 3120) image sensor with PureCel®Plus technology

datasheet (COB)
PRELIMINARY SPECIFICATION

version 1.14
march 2019

To learn more about OmniVision Technologies, visit www.ovt.com.

applications

- smart phones and feature phones
- PC multimedia
- tablets
- wearables

ordering information

- **OV13B10-GA5A-Z** (color, chip probing, 150 µm backgrinding, reconstructed wafer)

features

- 1.12 µm x 1.12 µm pixel
- optical size of 1/3.06"
- 33.25° CRA
- support for phase detection auto focus (PDAF)
- 13MP at 30 fps
- programmable controls for frame rate, mirror and flip, cropping, and windowing
- supports images sizes: 13 MP (4208x3120), 10 MP (4208x2368), 3 MP (2104x1560), 1080p and more
- support for output formats: 10-bit RAW RGB
- total embedded one-time programmable (OTP) memory: 512 bytes
- two-wire serial bus control (SCCB)
- MIPI serial output interface (1-, 2-lane, or 4-lane)
- two on-chip phase lock loops (PLLs)
- 2x binning support
- image quality controls: defect pixel correction (DPC) and automatic black level calibration (ABLC)
- suitable for module size of 8.5 x 8.5 x <5mm

key specifications (typical)

- **active array size:** 4208x3120
- **power supply:**
  - analog: 2.7 to 2.9V (2.8V nominal)
  - core: 1.14 to 1.26V (1.2V nominal)
  - I/O: 1.7 to 1.9V (1.8V nominal)
- **power requirements:**
  - active: 194mW
  - standby: 1mW
  - XSHUTDN: 1µW
- **temperature range:**
  - operating: -30°C to 85°C junction temperature (see **table 7-2**)
  - stable image: 0°C to 60°C junction temperature (see **table 7-2**)
- **output interface:** 4-lane MIPI serial output
- **output format:** 10-bit RGB RAW
- **lens size:** 1/3.06"
- **input clock frequency:** 6~64 MHz
- **lens chief ray angle:** 33.25° non-linear (see **figure 9-3**)
- **maximum image transfer rate:**
  - 13MP (4208x3120): 30 fps (see **table 2-1**)
  - 10MP (4208x2368): 30 fps (see **table 2-1**)
  - 3MP (2104x1560): 60 fps (see **table 2-1**)
  - 1080p (1920x1080): 60 fps (see **table 2-1**)
- **sensitivity:** 3700 e⁻/Lux-sec
- **max S/N ratio:** 36.5 dB
- **dynamic range:** 65 dB @ 1x gain
- **minimum exposure:** 4 lines
- **maximum exposure:** VTS-8
- **pixel size:** 1.12 µm x 1.12 µm
- **image area:** 4713.984 µm x 3499.776 µm
- **die dimensions:** 5412.6 µm x 4741.2 µm (COB), 5462.6 µm x 4791.2 µm (RW) (see **section 8** for details)

note COB refers to whole wafers with known good die and RW refers to singulated good die on a reconstructed wafer. Die size differs between COB and RW.

table of contents

list of figures

list of tables

1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pad numbers for the OV13B10 image sensor. The die information is shown in **section 8**.

figure 1-1 pad diagram

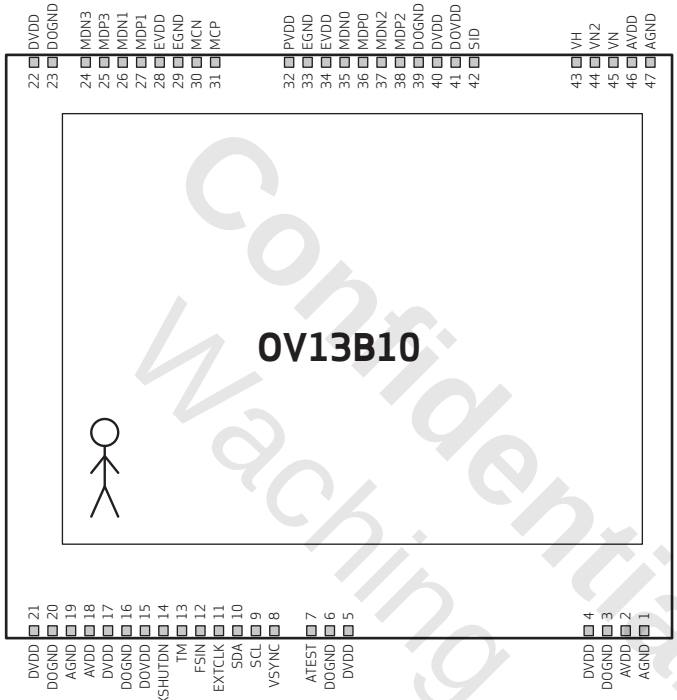


table 1-1 signal descriptions (sheet 1 of 3)

pad number	signal name	pad type	description
1	AGND	ground	ground for analog circuit
2	AVDD	power	power for analog circuit
3	DOGND	ground	ground for I/O circuit
4	DVDD	power	power for digital circuit
5	DVDD	power	power for digital circuit
6	DOGND	ground	ground for I/O circuit
7	ATEST	output	analog test pin 1

table 1-1 signal descriptions (sheet 2 of 3)

pad number	signal name	pad type	description
8	VSYNC	I/O	frame sync
9	SCL	input	SCCB input clock
10	SDA	I/O	SCCB data
11	EXTCLK	input	system clock input
12	FSIN	I/O	video output frame start signal
13	TM	input	test mode (scan chain active high with internal pull down resistor)
14	XSHUTDN	input	reset and power down (active low with pull down resistor)
15	DOVDD	power	power for I/O circuit
16	DOGND	ground	ground for I/O circuit
17	DVDD	power	power for digital circuit
18	AVDD	power	power for analog circuit
19	AGND	ground	ground for analog circuit
20	DOGND	ground	ground for I/O circuit
21	DVDD	power	power for digital circuit
22	DVDD	power	power for digital circuit
23	DOGND	ground	ground for I/O circuit
24	MDN3	output	MIPI data lane 3 negative output
25	MDP3	output	MIPI data lane 3 positive output
26	MDN1	output	MIPI data lane 1 negative output
27	MDP1	output	MIPI data lane 1 positive output
28	EVDD	power	power for MIPI/PLL circuit
29	EGND	ground	ground for MIPI/PLL circuit
30	MCN	output	MIPI clock lane negative output
31	MCP	output	MIPI clock lane positive output
32	PVDD	power	PLL analog power
33	EGND	ground	ground for MIPI/PLL circuit
34	EVDD	power	power for MIPI/PLL circuit
35	MDN0	output	MIPI data lane 0 negative output
36	MDP0	output	MIPI data lane 0 positive output
37	MDN2	output	MIPI data lane 2 negative output

table 1-1 signal descriptions (sheet 3 of 3)

pad number	signal name	pad type	description
38	MDP2	output	MIPI data lane 2 positive output
39	DOGND	ground	ground for I/O circuit
40	DVDD	power	power for digital circuit
41	DOVDD	power	power for I/O circuit
42	SID	input	SCCB ID select
43	VH	input	reference
44	VN2	input	reference
45	VN	input	reference
46	AVDD	power	power for analog circuit
47	AGND	ground	ground for analog circuit

table 1-2 configuration under various conditions (sheet 1 of 2)

pad	signal name	XSHUTDN[a]	after XSHUTDN release[b]	software standby
8	VSYNC	high-z	high-z	high-z (configurable)
9	SCL	input	input	input
10	SDA	open drain	I/O	I/O
11	EXTCLK	input	input	input
12	FSIN	high-z	high-z	high-z (configurable)
13	TM	input	input	input
14	XSHUTDN	input	input	input
24	MDN3	high-z	high	high by default (configurable)
25	MDP3	high-z	high	high by default (configurable)
26	MDN1	high-z	high	high by default (configurable)
27	MDP1	high-z	high	high by default (configurable)
30	MCN	high-z	high	high by default (configurable)
31	MCP	high-z	high	high by default (configurable)
35	MDN0	high-z	high	high by default (configurable)
36	MDP0	high-z	high	high by default (configurable)

table 1-2 configuration under various conditions (sheet 2 of 2)

pad	signal name	XSHUTDN[a]	after XSHUTDN release[b]	software standby
37	MDN2	high-z	high	high by default (configurable)
38	MDP2	high-z	high	high by default (configurable)
42	SID	input	input	input

a. XSHUTDN = 0

b. XSHUTDN from 0 to 1

table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

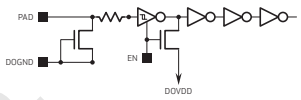
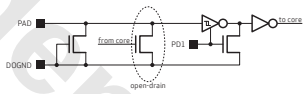
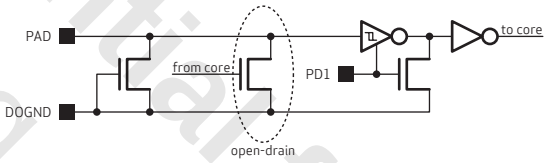
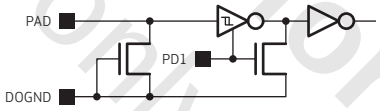
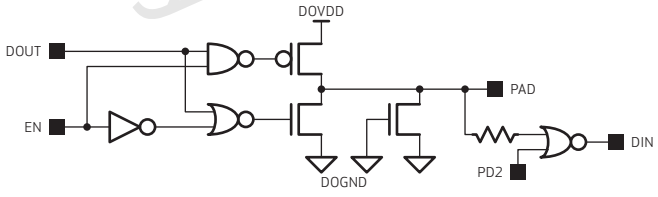
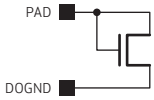
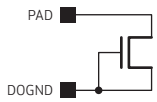
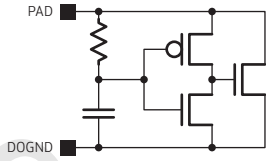
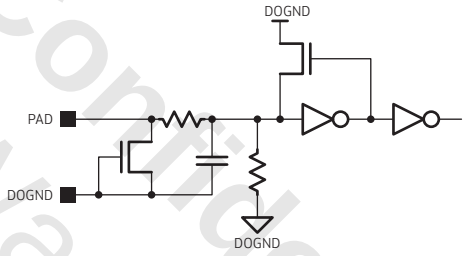
symbol	equivalent circuit
EXTCLK	
SID	
SDA	
SCL	
FSIN, VSYNC	
VN, VN2	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
MDP3, MDP2, MDP1, MDP0, MDN3, MDN2, MDN1, MDN0, MCP, MCN, EGND, AGND, DOGND, VH	
AVDD, EVDD, DVDD, DOVDD, PVDD	
XSHUTDN, TM	

2 system level description

2.1 overview

The OV13B10 RAW RGB PureCel®Plus image sensor is a high performance, 1/3.06-inch, CMOS, image sensor that delivers 13 megapixels (4208x3120) at 30 fps. It provides full-frame, sub-sampled, and windowed 10-bit MIPI images in various formats via control of the Serial Camera Control Bus (SCCB) interface.

The OV13B10 has a 13 megapixel image array capable of operating at up to 30 frames per second (fps) in 10-bit resolution with complete user control over image quality, formatting and output data transfer. Some image processing functions, such as defective pixel correction, etc., are programmable through the SCCB interface.

In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

For customized information purposes, the OV13B10 includes 4k bits (512 bytes) of one-time programmable (OTP) memory (TBD bytes are reserved for OmniVision and TBD bytes are reserved for customer use). The OV13B10 has a MIPI interface of up to four lanes.

2.1.1 identifying the sensor's revision ID

For the OV13B10, the sensor's revision ID can be read out from the one-time programmable (OTP) memory. To read out data from OTP, perform the following steps:

```
6C 0100 01
6C 3D84 00
6C 3D81 01
```

Then, verify that register 0x7000 = 0x01, register 0x7001 = 0x3B, and register 0x7002 = 0x10.

2.2 architecture

The OV13B10 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV13B10 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, pre-charging and sampling rows of the array sequentially. In the time between pre-charging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC, which outputs 10-bit data for each pixel in the array.

figure 2-1 OV13B10 block diagram

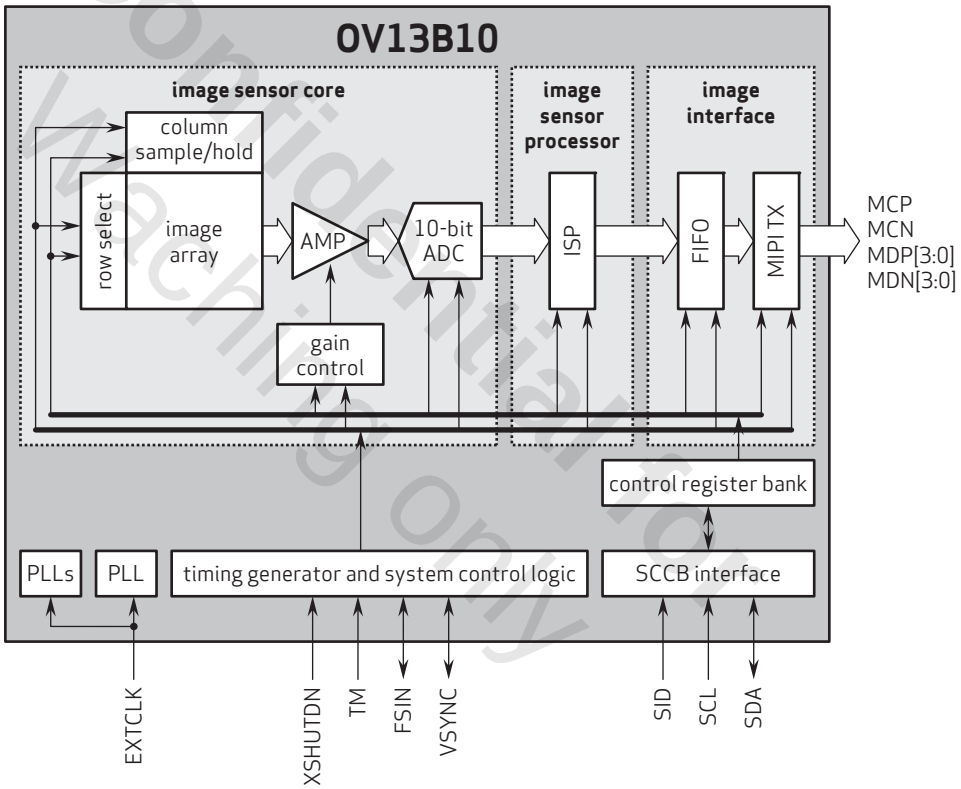
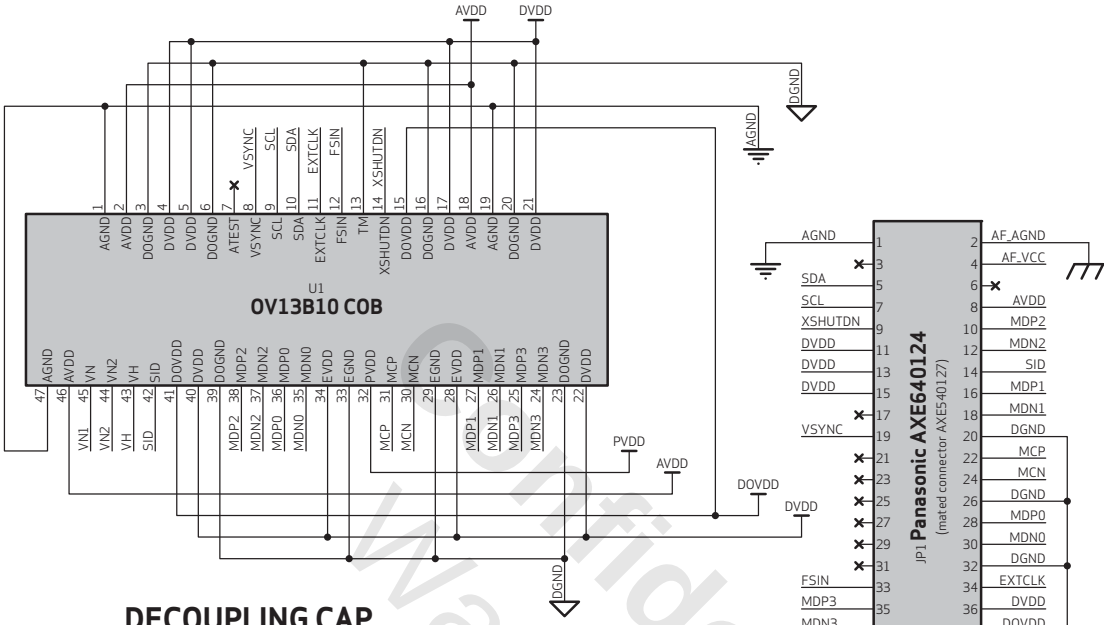


figure 2-2 OV13B10 reference design schematic



note 1 XSHUTDOWN (XSHUTDN) should be connected to DOVDD outside of module if unused.

note 2 for other pins, such as FSIN, VSYNC, if unused, can leave floating.

note 3 AVDD is 2.7-2.9V for sensor analog power (clean).

note 4 DOVDD is 1.62-1.98V for sensor digital IO power (clean).

note 5 DVDD is 1.14-1.26V of sensor digital core power (clean).

note 6 sensor AGND and DGND should be separated and connected to a single point outside PCB (do not connect inside module).

note 7 capacitors should be close to their related sensor pins.

note 8 MCP and MCN are MIPI clock lane positive and negative outputs.
MDPx and MDNx are MIPI data lane positive and negative outputs.

note 9 traces of MCP, MCN, MDPx and MDNx should have same or similar length.
differential impedance of clock pair and data pair transmission lines should be controlled at 100 Ohm.

note 10 AF_VCC and AF_AGND is power supply for auto focus related circuitry.
AF_VCC can be 2.8-3.3V.

2.3 format and frame

The OV13B10 supports RAW RGB output with one/two/four lane MIPI interface.

table 2-1 format and frame rate

format	resolution	frame rate	methodology	10-bit MIPI data rate (default)
13.2 Mpixel	4208 x 3120	30 fps	full resolution (4:3)	4-lane @ 1120 Mbps/lane
10 Mpixel	4208 x 2368	30 fps	crop (16:9)	4-lane @ 1120 Mbps/lane
3.3 Mpixel	2104 x 1560	60 fps	bin2/skip2	4-lane @ 560 Mbps/lane
1080p	1920 x 1080	60 fps	bin2 + crop	4-lane @ 560 Mbps/lane
720p	1280 x 720	120 fps	bin2 + crop	4-lane @ 560 Mbps/lane

2.4 I/O control

The OV13B10 can configure its I/O pads as an input or output. For the output signal, it follows one of two paths: either from the data path or from register control.

table 2-2 I/O control registers

function	register	description
output drive capability control	0x3663	Bit[6:5]: I/O pad drive capability 00: 1x 01: 2x 10: 3x 11: 4x
FSIN I/O control	0x3002	Bit[7]: FSIN output enable 0: input 1: output
VSYNC I/O control	0x3002	Bit[6]: VSYNC output enable 0: input 1: output
FSIN output select	0x3010	Bit[7]: enable FSIN as GPIO controlled by register
VSYNC output select	0x3010	Bit[6]: enable VSYNC as GPIO controlled by register
FSIN output value	0x3008	Bit[7]: register control FSIN output
VSYNC output value	0x3008	Bit[6]: register control VSYNC output

2.5 MIPI interface

The OV13B10 supports a MIPI interface of up to 4-lanes. The MIPI interface can be configured for 1/2/4-lane and each lane is capable of a data transfer rate of up to 1.2 Gbps.

2.6 power management

The power up sequence will differ based on the system power configuration (XSHUTDN). OmniVision recommends cutting off all power supplies, including the external DVDD, when the sensor is not in use.

2.6.1 power up sequence

To avoid any glitch from a strong external noise source, OmniVision recommends controlling XSHUTDN by GPIO.

Whether or not XSHUTDN is controlled by GPIO, XSHUTDN rising cannot occur before AVDD, DVDD and DOVDD.

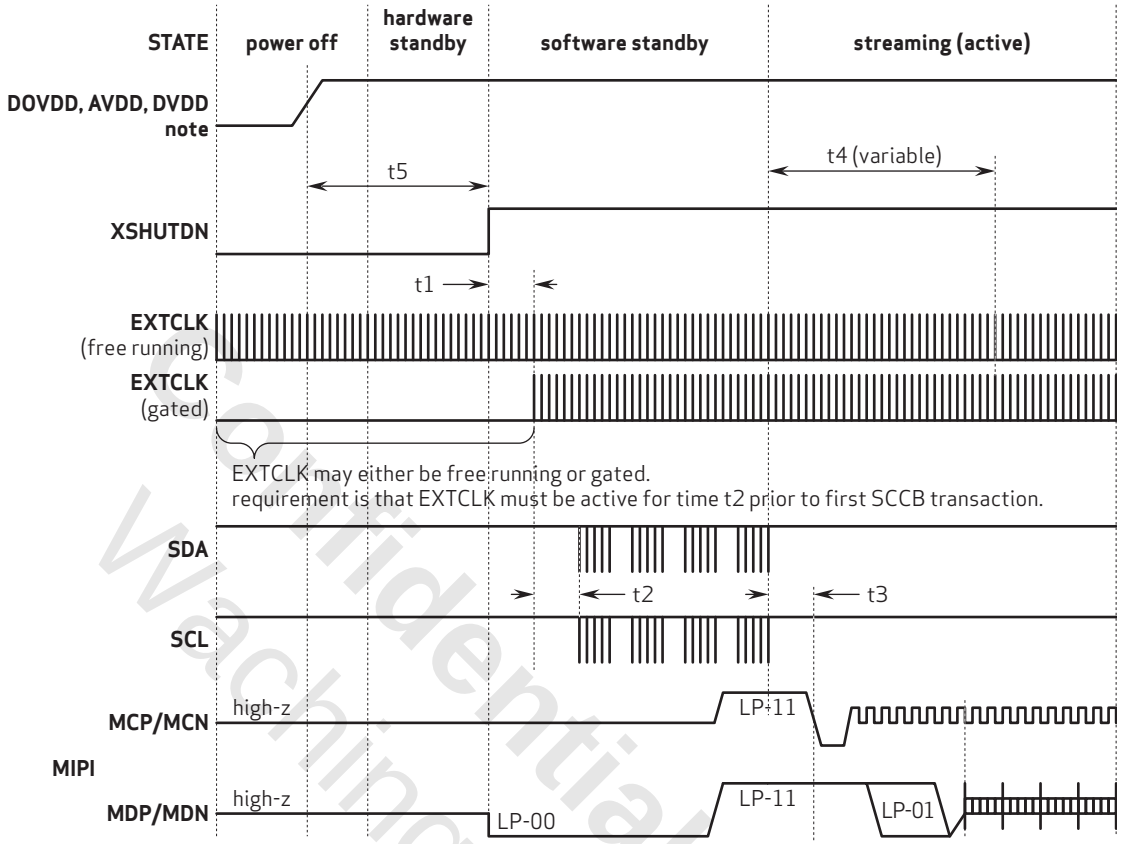
table 2-3 power up sequence

XSHUTDN	power up sequence requirement
GPIO	Refer to **figure 2-3** 1. DOVDD, AVDD, and DVDD can rise in any order 2. XSHUTDN rising must occur after AVDD, DOVDD and DVDD are stable

table 2-4 power up sequence timing constraints

constraint	label	min	max	unit
XSHUTDN rising – system ready	t1	5		ms
minimum number of EXTCLK cycles prior to first SCCB transaction	t2	8192		EXTCLK cycles
MIPI clock startup time	t3		8192	EXTCLK cycles
entering streaming mode – first frame start sequence (variable)	t4	delay related to output frame rate and line timing		lines
AVDD, DOVDD or DVDD, whichever is last – XSHUTDN rising	t5	0	∞	ns

figure 2-3 power up sequence



note DOVDD, AVDD and DVDD may rise in any order

2.6.2 power down sequence

Pull XSHUTDN low to set the sensor into power down mode. The digital and analog supply voltages can be cut off in any order (e.g., DOVDD, DVDD, then AVDD or AVDD, DVDD, then DOVDD). Similar to the power up sequence, the EXTCLK input clock may be either gated or continuous. To avoid bad frames from MIPI, OmniVision recommends setting the sensor into sleep mode in inter frame first before sending the sensor into power down mode by setting register 0x3021[6:5] = 2'b00 and register 0x0100 = 0x00.

table 2-5 power down sequence

XSHUTDN	power down sequence requirement
GPIO	Refer to **figure 2-5** 1. Software standby recommended 2. Pull XSHUTDN low for minimum power consumption 3. Pull AVDD, DVDD, and DOVDD low in any order

table 2-6 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for MIPI end code before entering software for standby; otherwise, enter software standby mode immediately		
minimum of EXTCLK cycles after last SCCB transaction or MIPI frame end	t1	512		EXTCLK cycles
last SCCB transaction or MIPI frame end – XSHUTDN falling	t2	512		EXTCLK cycles
XSHUTDN falling – AVDD/DVDD or DOVDD falling, whichever is first	t3	0.0		ns

figure 2-4 software standby sequence

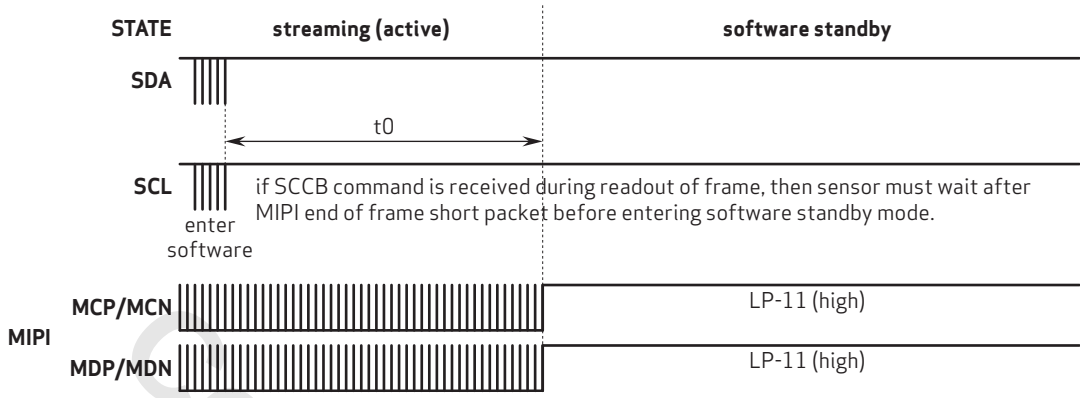
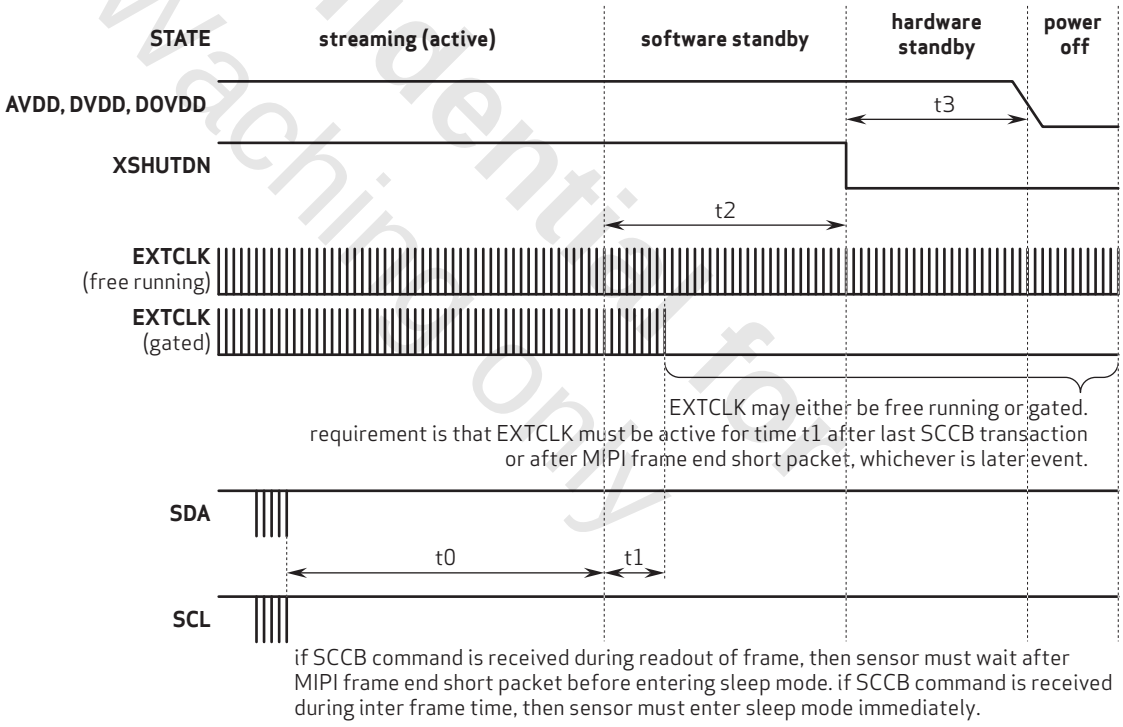


figure 2-5 power down sequence



2.7 reset

The whole chip will be reset during power up. Manually applying a hardware reset (XSHUTDN = 0) upon power up is recommended even though the on-chip power up reset is included. The hardware reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 2 ms.

2.7.1 power ON reset

The power on reset can be controlled from an external pin. Additionally, this sensor generates a power on reset after the core power becomes stable.

2.7.2 software reset

When register 0x0103[0] is configured as 1, all registers are reset to default value.

2.8 standby mode

Two suspend modes are available for the OV13B10:

- hardware standby
- software standby

2.8.1 hardware standby

If XSHUTDN is tied to low, it will initiate hardware standby mode. In this mode, the total power consumption will be less than 100 µW.

2.8.2 software standby

Executing a software power down (0x0100[0]) through the SCCB interface suspends internal circuit activity, but does not halt the device clock. All register content is maintained in standby mode. During resume state, all registers are restored to their original values.

table 2-7 hardware and standby description

mode	description
hardware standby with XSHUTDN	1. Enabled by pulling XSHUTDN low 2. Power down all blocks 3. Register values are reset to default values 4. No SCCB communication 5. Minimum power consumption
software standby	1. Default mode after power on reset 2. Power down all blocks except SCCB 3. Register values are maintained 4. SCCB communication is available 5. Low power consumption 6. GPIO can be configured as high/low/tri-state

2.9 system clock control

The OV13B10 has two on-chip PLLs which generate the system clock from a 6~64 MHz input clock. A programmable clock divider is provided to generate different frequencies for the system. PLL settings can only be changed during sensor software standby mode (0x0100 = 0).

2.9.1 PLL1

PLL1 generates a default 140 MHz pixel clock and 560 MHz MIPI serial clock from a 6~64 MHz input clock. The VCO range is from 500 MHz to 1500 MHz.

2.9.2 PLL2

PLL2 generates a default 112 MHz system clock from a 6~64 MHz input clock. The VCO range is from 500 MHz to 1500 MHz. PLL2 is only used for sensor timing and should not be adjusted by the customer.

figure 2-6 clock scheme

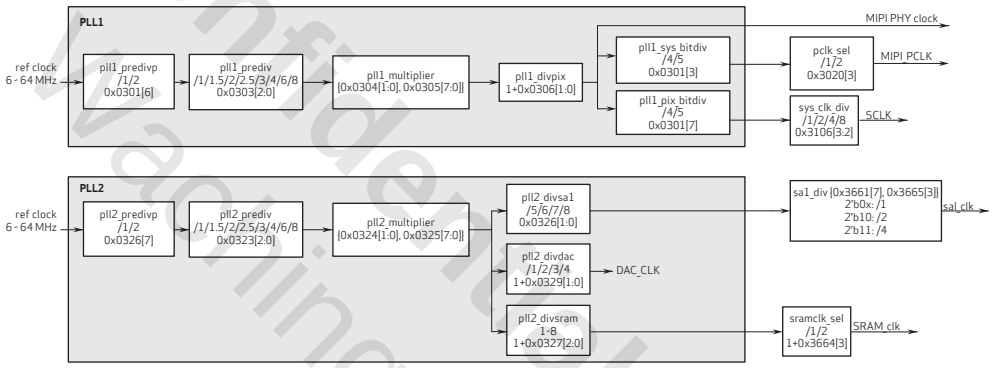


table 2-8 PLL control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x0301	PLL_CTRL_1	0x80	RW	Bit[7]: pll1_pix_bitdiv 0: /4 1: /5 Bit[6]: pll1_predivp 0: /1 1: /2 Bit[3]: pll1_sys_bitdiv 0: /4 1: /5

table 2-8 PLL control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x0303	PLL_CTRL_3	0x01	RW	Bit[2:0]: pll1_prediv 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0304	PLL_CTRL_4	0x00	RW	Bit[1:0]: pll1_multiplier[9:8]
0x0305	PLL_CTRL_5	0x46	RW	Bit[7:0]: pll1_multiplier[7:0]
0x0306	PLL_CTRL_6	0x00	RW	Bit[1:0]: pll1_divpix 00: /1 01: /2 10: /3 11: /4
0x0323	PLL_CTRL_23	0x00	RW	Bit[2:0]: pll2_prediv 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0324	PLL_CTRL_24	0x00	RW	Bit[1:0]: pll2_multiplier[9:8]
0x0325	PLL_CTRL_25	0x38	RW	Bit[7:0]: pll2_multiplier[7:0]
0x0326	PLL_CTRL_26	0x01	RW	Bit[7]: pll2_predivp 0: /1 1: /2 Bit[1:0]: pll2_divsa1 00: /5 01: /6 10: /7 11: /8
0x0327	PLL_CTRL_27	0x05	RW	Bit[2:0]: pll2_divsram Control bit value = bit[2:0] + 1
0x0329	PLL_CTRL_29	0x01	RW	Bit[1:0]: pll2_divdac 00: /1 01: /2 10: /3 11: /4

table 2-8 PLL control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3020	CLOCK SEL	0x9B	RW	Bit[3]: pclk_sel 0: /1 1: /2
0x3106	SRB HOST INPUT DIS	0x15	RW	Bit[3:2]: sys_clk_div 00: /1 01: /2 10: /4 11: /8
0x3664	CORE TOP REG04	0x71	RW	Bit[3]: sramclk_sel 0: pll2_sram_clk_real comes from pll2_sram_clk2x 1: pll2_sram_clk_real comes from pll1_sram_clk1x

table 2-9 sample PLL configuration

control name	address	input clock (EXTCLK)	
		24 MHz	6 MHz
PLL1_PREDIVP	0x0301[6]	0x0	0x0
PLL1_PREDIV	0x0303[2:0]	0x1	0x1
PLL1_MULTIPLIER	{0x0304[1:0], 0x0305[7:0]}	0x46	0x118
PLL1_DIVPIX	0x0306[1:0]	0x0	0x0
PLL1_PIX_BITDIV	0x0301[3]	0x0	0x0
PLL1_SYS_BITDIV	0x0301[7]	0x1	0x1
PLL2_PREDIVP	0x3026[7]	0x0	0x0
PLL2_PREDIV	0x0323[2:0]	0x0	0x0
PLL2_MULTIPLIER	{0x0324[1:0], 0x0325[7:0]}	0x38	0x38
PLL2_SA1_DIV	0x0326[1:0]	0x1	0x1
PLL2_SRAMDIV	0x0327[2:0]	0x5	0x5
PLL_PCLK_DIV	0x3020[3]	–	–
SYS_CLK_DIV	0x3106[3:2]	–	–
SRAMCLK_SEL	0x3664[3]	–	–
SCLK	–	112 MHz	112 MHz
PHY_SCLK	–	1120 MHz	1120 MHz
MIPI_PCLK	–	140 MHz	140 MHz

2.10 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

In the OV13B10, the SCCB ID is controlled by the SID pin and can be programmed. If SID is low, the sensor's SCCB address comes from register 0x3003, which has a default value of 0x6C for write (0x6D for read). If SID is high, the sensor's SCCB address comes from register 0x3004, which has a default value of 0x20 for write (0x21 for read). There is an alternative ID in register 0x3005, which has a default value of 0x42. The alternative ID works on both SID high or low.

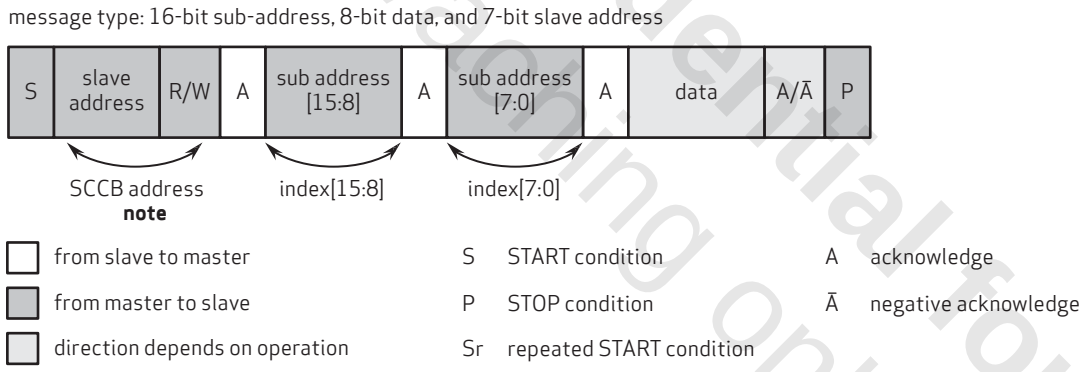
2.10.1 data transfer protocol

Data transfer of the OV13B10 follows the SCCB protocol.

2.10.2 message format

The OV13B10 supports the message format shown in **figure 2-7**. The repeated START (Sr) condition is not shown in **figure 2-8**, but is shown in **figure 2-9** and **figure 2-10**.

figure 2-7 message type



note slave address must be 0x36 for SCCB write address to be 0x6C and for SCCB read address to be 0x6D

2.10.3 read / write operation

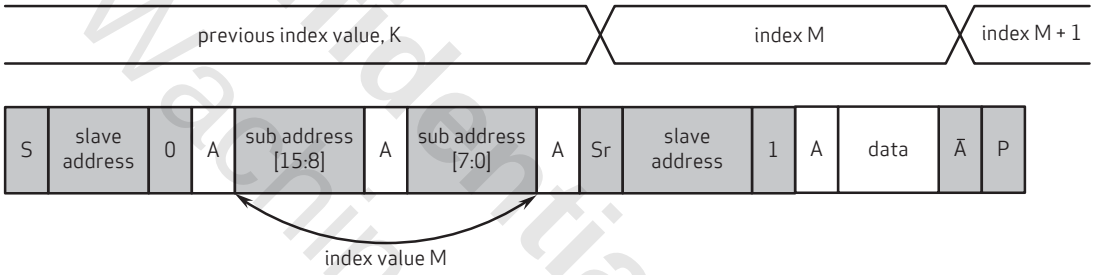
The OV13B10 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

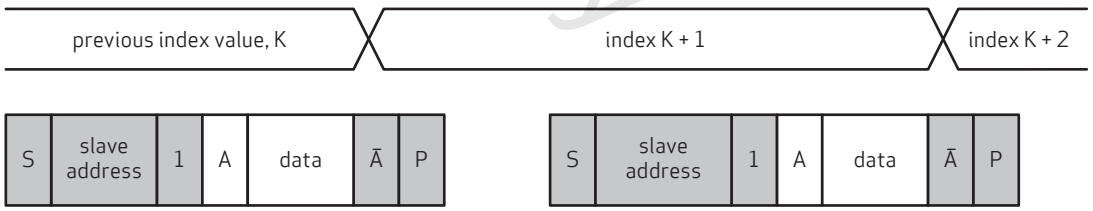
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 2-8**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-8 SCCB single read from random location



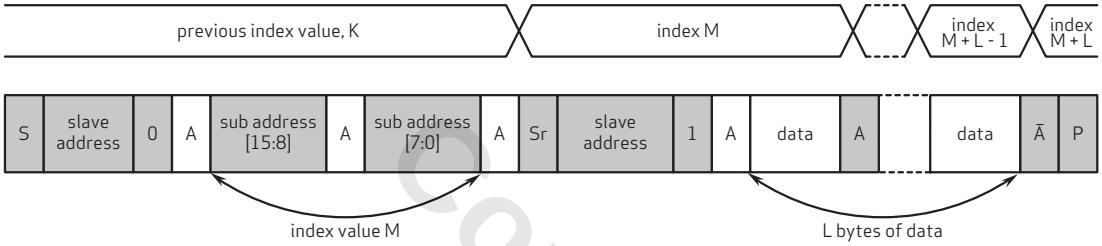
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 2-9**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-9 SCCB single read from current location



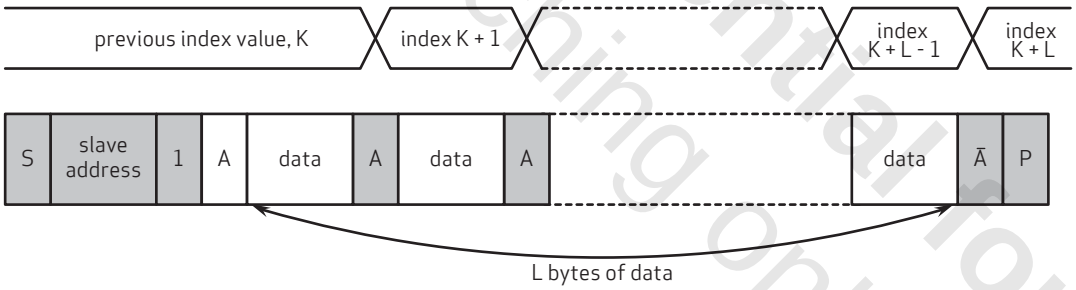
The sequential read from a random location is illustrated in **figure 2-10**. The master performs a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-10 SCCB sequential read from random location



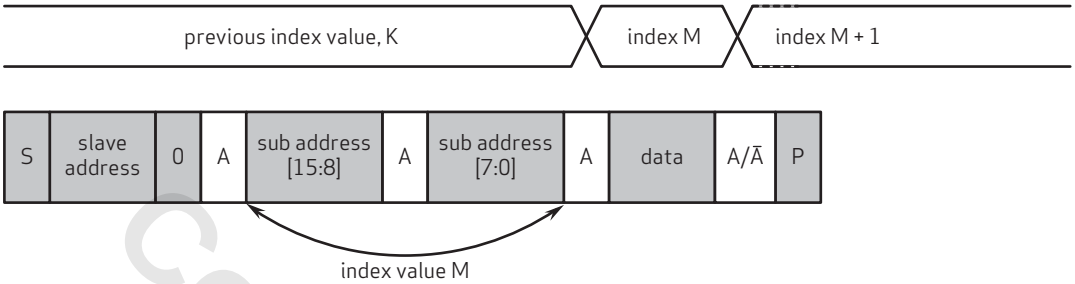
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation as shown in **figure 2-11**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-11 SCCB sequential read from current location



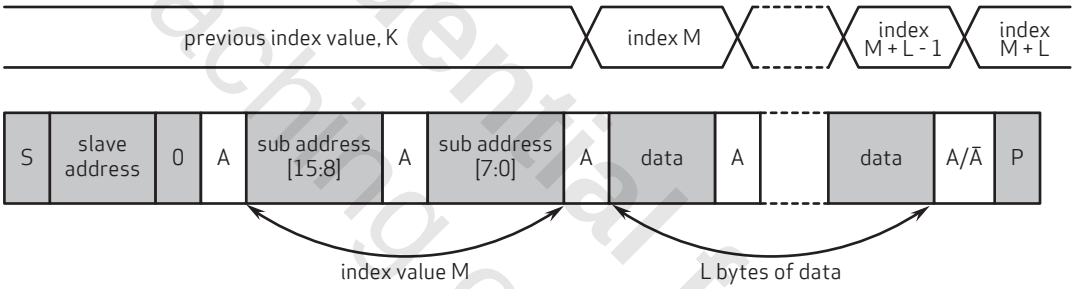
The write operation to a random location is illustrated in **figure 2-12**. The master issues a write operation to the slave, and sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-12 SCCB single write to random location



The sequential write is illustrated in **figure 2-13**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-13 SCCB sequential write to random location



2.10.4 SCCB timing

figure 2-14 SCCB interface timing

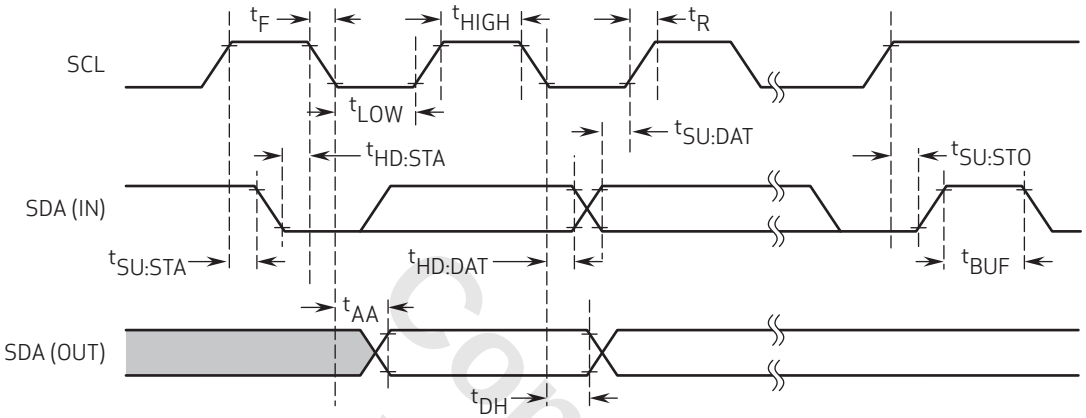


table 2-10 SCCB interface timing specifications[a]

symbol	parameter	400kHz mode		1000kHz mode[b]		unit
		min	max	min	max	
f_{SCL}	clock frequency		400		1000	kHz
t_{LOW}	clock low period	1.3		0.5		µs
t_{HIGH}	clock high period	0.6		0.26		µs
t_{AA}	SCL low to data out valid	0.1	0.9	0.05	0.45	µs
t_{BUF}	bus free time before new start	1.3		0.5		µs
$t_{HD:STA}$	start condition hold time	0.6		0.26		µs
$t_{SU:STA}$	start condition setup time	0.6		0.26		µs
$t_{HD:DAT}$	data in hold time	0		0		µs
$t_{SU:DAT}$	data in setup time	0.1		0.05		µs
$t_{SU:STO}$	stop condition setup time	0.6		0.26		µs
t_R, t_F	SCCB rise/fall times		0.3		0.12	µs
t_{DH}	data out hold time	0.05		0		µs

a. timing measurement shown at beginning of rising edge and/or end of falling edge signifies 30%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge and/or beginning of falling edge signifies 70%

b. when input clock > 10 MHz

2.11 group write

Group write is supported in order to update a group of registers (except 0x31xx) in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary. If more than one group is going to be launched, the second group cannot be recorded or launched before the first group has effectively been launched.

The OV13B10 supports up to four groups. These groups share 512 bytes of memory and the size of each group is programmable by adjusting the start address.

table 2-11 group hold registers

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch 1110: Fast group launch Others: Reserved Bit[3:0]: Group ID 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3 Others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	When 0x320B[7] = 1 Bit[6:5]: Group number that group will switch back to after launch group 0 in auto switch mode Bit[4:0]: grp0_frms Number of frames stay in group 0 before auto switch to group defined by 0x3209[6:5] When 0x320B[2] = 1 Bit[7:0]: Number of frames stay in group 0 before auto switch to group defined by 0x320B[1:0]
0x320A	GRP1_PERIOD	0x00	RW	Bit[7:0]: Number of frames stay in second group in context switch mode defined by 0x320B[1:0] (works only when 0x320B[2] = 1)
0x320B	GRP_SWCTRL	0x11	RW	Bit[7]: auto_sw Auto launch mode enable Bit[4]: frame_cnt_trig 0: EOF as frame count trigger 1: Group write as frame count trigger Bit[3]: group_switch_repeat Bit[2]: context_en Contact switch mode enable Bit[1:0]: Second group selection

2.11.1 hold

After the groups are configured, users can perform a hold operation to store register settings into the SRAM of each group. The hold of each group starts and ends with control register 0x3208. The lower 4 bits of register 0x3208 control which group to access, and the upper 4 bits control the start (0x0: hold start) and end (0x1: hold end) of the hold operation.

The example setting below shows the sequence to hold group 0:

```
6C  3208  00    group 0 hold start
6C  3800  11    first register into group 0
6C  3911  22    second register into group 0
6C  3208  10    group 0 hold end
```

2.11.2 launch

After the contents of each group are defined in the hold operation, all registers belonging to each group are stored in SRAM and ready to be written into target registers (i.e., launch of that group).

There are five launch modes as described in sections **section 2.11.2.1** to **section 2.11.2.5**.

2.11.2.1 launch mode 1 – quick manual launch

Manual launch is enabled by setting register 0x320B to 0.

Quick manual launch is achieved by writing to control register 0x3208. The value written into this register is 0xEX, the upper 4 bits (0xE) are the quick launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 0, they just write the value 0xE0 to register 0x3208, then the contents of group 0 will be written to the target registers immediately after the sensor receives this command through the SCCB. Below is a setting example.

```
6C  3208  E0    quick launch group 0
```

2.11.2.2 launch mode 2 – delay manual launch

Delay manual launch is achieved by writing to register 0x3208. The value written into this register is 0xAX, where the upper 4 bits (0xA) are the delay launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 1, they just write the value 0xA1 to register 0x3208, then the contents of group 1 will be written to the target registers. The difference with mode 1 is that the writing will wait for some internally defined time spot in vertical blanking; thus delaying it. Below is a setting example.

```
6C  3208  A1    delay launch group 1
```

2.11.2.3 launch mode 3 – quick auto launch

Quick auto launch works like mode 1, but the difference is it will return to a specified group automatically. This is controlled by register 0x3209. Bit[6:5] controls which group to return to and Bit[4:0] controls how many frames to stay before returning. The auto launch enable bit is bit[7] of register 0x320B. The operation can be better understood with an example setting:

```
20 3209 44 ;Bit[6:5]: 2, return to group 2, Bit[4:0]: 4: stay 4 frames
20 320B 80 ; auto launch on
20 3208 E0 ;quick launch group 0
```

In this example, the sensor will quick launch group 0, stay at group 0 for 4 frames, and then return to group 2 after that.

2.11.2.4 launch mode 4 – delay auto launch

Delay auto launch works like mode 2 during the delay launch operation and like mode 3 during the return operation.

The operation can be better understood with an example setting:

```
20 3209 44 ;bit[6:5]: 2, return to group 2, Bit [4:0]: 4: stay 4 frames
20 320B 80 ; auto launch on
20 3208 A0 ;delay launch group 0
```

In this example, the sensor will delay launch group 0, stay at group 0 for 4 frames, and then return to group 2 after that.

2.11.2.5 launch mode 5 – repeat launch

Repeat launch is controlled by registers 0x3209, 0x320A, and 0x320B. In this mode, the launch is repeated automatically between the first group (must be group 0) and the second group (could be any one of group 1-3, which is specified by register 0x320B[1:0]). The register 0x3209 defines how many frames to stay at group 0 and register 0x320A defines how many frames to stay at the second group.

The operation can be better understood with an example setting:

```
20 3209 02 ; bit[7:0]: 2, stay 2 frames in group 0
20 320A 03 ; bit[7]: 3, stay 3 frames in the second group
20 320B 0E ; bit[3:2]: 3, repeat launch on, Bit[1:0]: 2,second group select: group 2
20 3208 A0 ; always use a0 for repeat launch
```

In this example, the sensor will delay launch group 0, stay at group 0 for 2 frames, then switch to group 2 for 3 frames, then back to group 0 for 2 frames, then switch to group 2 for 3 frames and repeat.

3 block level description

3.1 pixel array structure

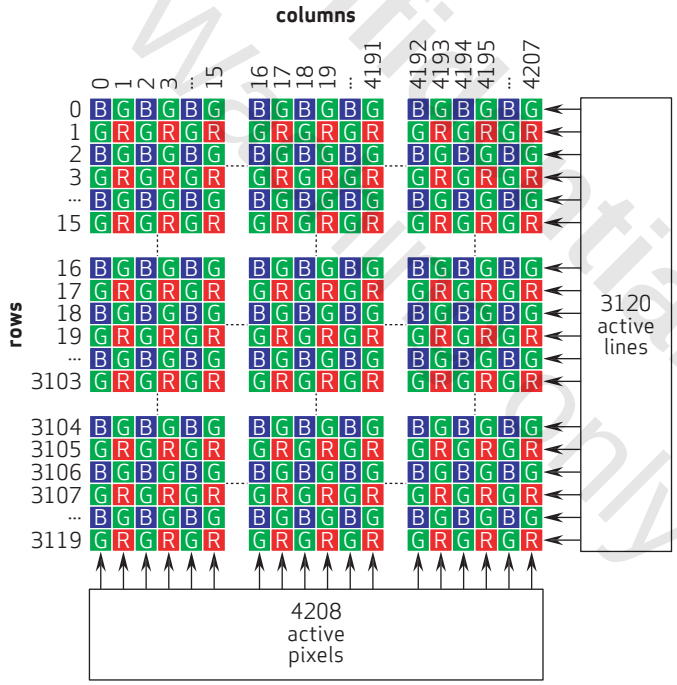
The OV13B10 sensor has an image array of 4224 columns by 3136 rows (13,246,464 pixels including 32 black lines).

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 13,246,464 pixels, 13,128,960 (4208x3120) are active pixels and can be output. **figure 3-1** shows the sensor output pattern.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

Exposure time is controlled by registers {0x3500, 0x3501, 0x3502}. Maximum exposure time is VTS-8 and minimum exposure time is 4 lines.

figure 3-1 sensor output pattern (4208x3120)



3.2 subsampling

The OV13B10 supports a binning mode to provide a lower resolution output while maintaining the field of view. With binning mode ON, the voltage levels of adjacent pixels (of the same color) are averaged before being sent to the ADC. The OV13B10 supports 2x2 binning, which is illustrated in **figure 3-2**, where the voltage levels of four adjacent same-color pixels are averaged.

figure 3-2 example of 2x2 binning

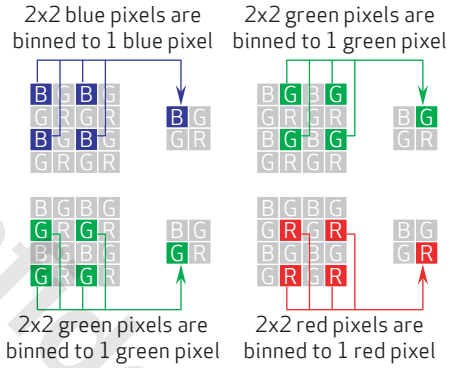


table 3-1 binning-related registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3820	FORMAT1	0x80	RW	Bit[5]: Black line vertical flip control 0: Normal 1: Vertical flip Bit[4]: Image vertical flip enable 0: Normal 1: Vertical flip Bit[3]: Image horizontal mirror disable 0: Image horizontal mirror enable 1: Normal Bit[2]: hbin4_o Bit[1]: hbin2_o Bit[0]: vbinf_o
0x3814	X INC ODD	0x01	RW	Bit[4:0]: x_odd_inc
0x3815	X INC EVEN	0x01	RW	Bit[4:0]: x_even_inc
0x382A	VTS ADJUST	0x00	RW	Bit[7:0]: man_vts_adj_val[15:8]
0x382B	VTS ADJUST	0x08	RW	Bit[7:0]: man_vts_adj_val[7:0]

table 3-1 binning-related registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4501	R1	0x00	RW	Bit[5:4]: r_hbin4_opt 00: Average of 4 pixels 01: Summary of 4 pixels 10: Select first bin2 pixel 11: Select last bin2 pixel Bit[3:2]: r_hbin2_opt 00: Average 01: Summary 10: Select first pixel 11: Select last pixel

3.3 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

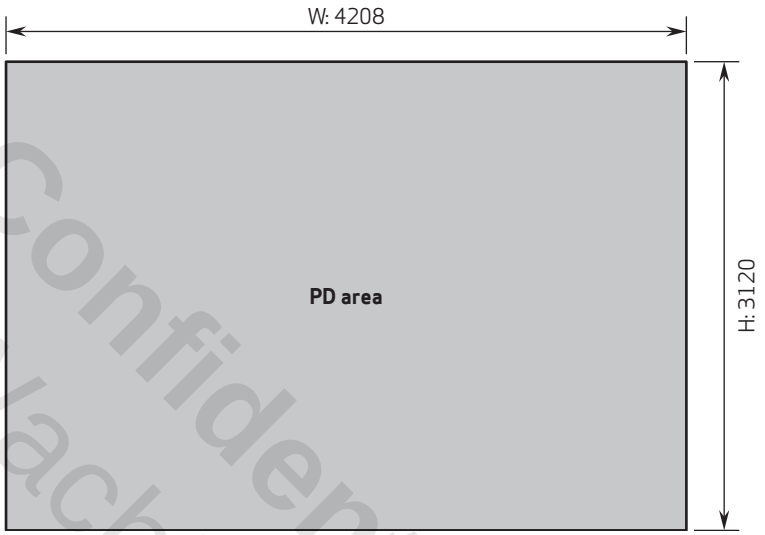
3.4 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC.

3.5 PD pixel arrangement

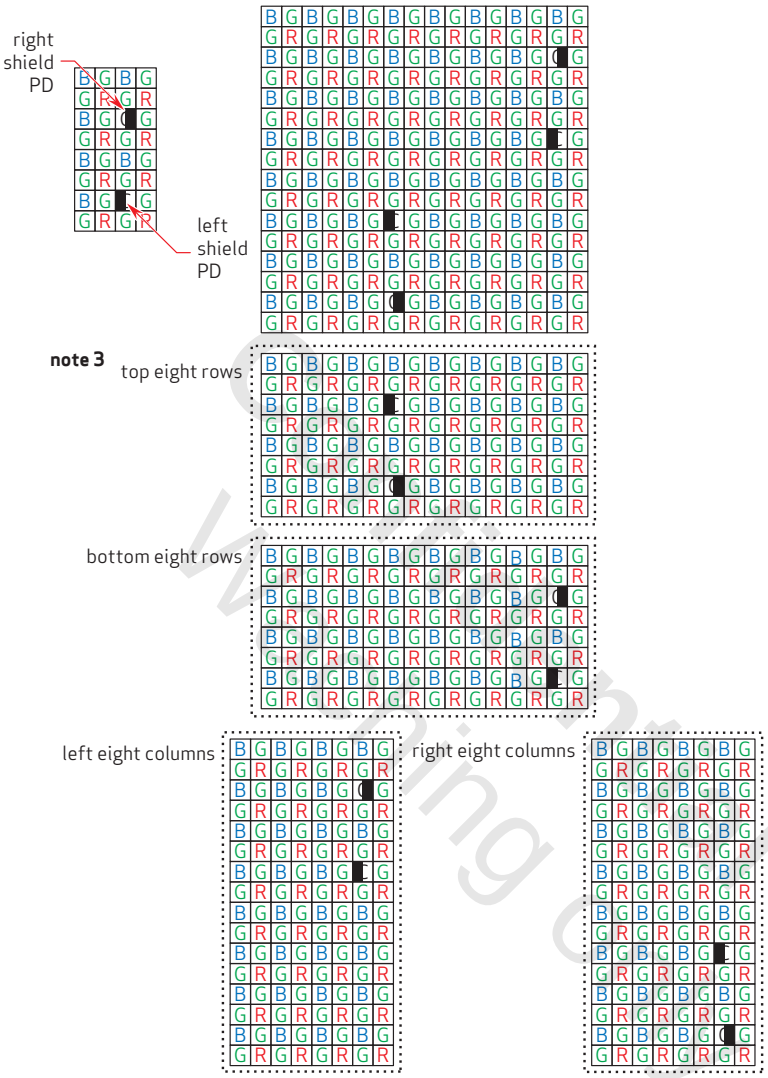
PD pixels are evenly arranged in the PD area. The PD pixel amount is 205,140, which is about 100% PD coverage for full resolution (4208x3120). The OV13B10 only supports type 3 PD format (PD in the output format).

figure 3-3 PD pixel arrangement



The full size PD pattern is evenly placed in a 16x16 PD area.

figure 3-4 PD pattern



note 1 first 16x16 pattern location is (8, 8) for 4208x3120

note 2 PD pixel is on B location, but is a C (clear) pixel

note 3 PD pattern is 16x16. PD patterns are symmetrically aligned from array center. For 4208x3120, top eight rows, bottom eight rows, left eight columns and right eight columns are shown above.

note 4 sensor is in correct orientation for correct image with normal sensor setting (see chapter 9 for correct orientation)

4 image sensor core digital functions

4.1 mirror and flip

The OV13B10 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	FORMAT1	0x80	RW	Bit[5]: Black line vertical flip control 0: Normal 1: Vertical flip Bit[4]: Image vertical flip enable 0: Normal 1: Vertical flip Bit[3]: Image horizontal mirror disable 0: Image horizontal mirror enable 1: Normal Bit[2]: hbin4_o Bit[1]: hbin2_o Bit[0]: vbinf_o

4.2 image cropping and windowing

An image cropping area is defined by four parameters, horizontal start (HS), horizontal end (HE), vertical start (VS), and vertical end (VE). By properly setting the parameters, any portion within the sensor array size can output as a visible area. A smaller cropping size may achieve a higher frame rate. Windowing is achieved by masking off the pixels outside of the window, defined by H_win_off and V_win_off control; thus, the original timing is not affected.

figure 4-2 image cropping and windowing

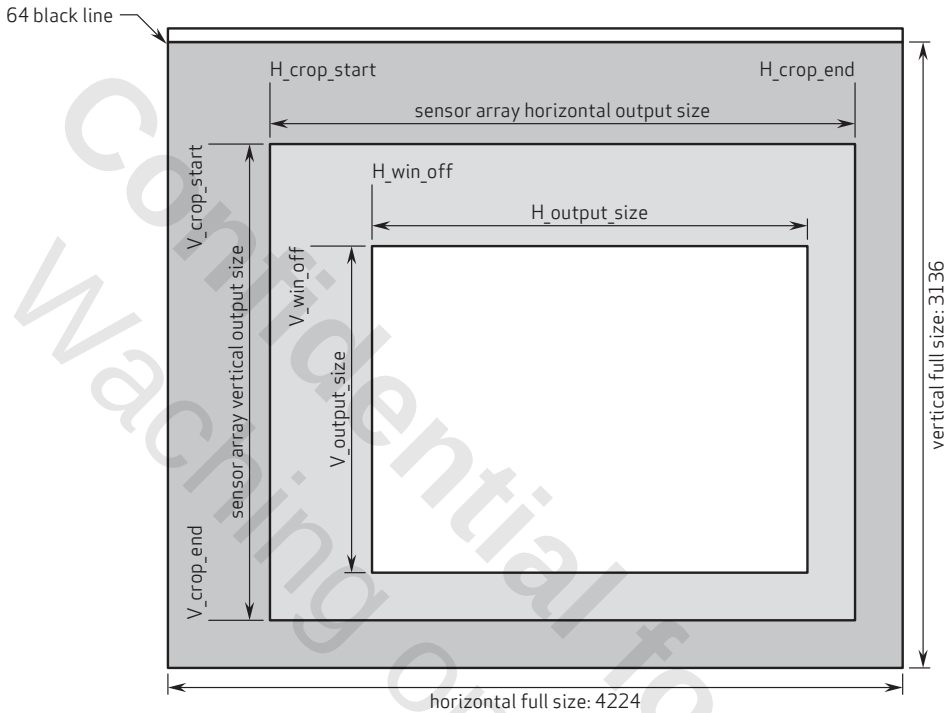


table 4-2 image cropping and windowing control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[15:8] Array horizontal start point
0x3801	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point
0x3802	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[15:8] Array vertical start point
0x3803	Y ADDR START	0x08	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point

table 4-2 image cropping and windowing control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3804	X ADDR END	0x10	RW	Bit[7:0]: x_addr_end[15:8] Array horizontal end point
0x3805	X ADDR END	0x8F	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point
0x3806	Y ADDR END	0x0C	RW	Bit[7:0]: y_addr_end[15:8] Array vertical end point
0x3807	Y ADDR END	0x47	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point
0x3808	X OUTPUT SIZE	0x10	RW	Bit[7:0]: x_output_size[15:8] ISP horizontal output width
0x3809	X OUTPUT SIZE	0x70	RW	Bit[7:0]: x_output_size[7:0] ISP horizontal output width
0x380A	Y OUTPUT SIZE	0x0C	RW	Bit[7:0]: y_output_size[15:8] ISP vertical output height
0x380B	Y OUTPUT SIZE	0x30	RW	Bit[7:0]: y_output_size[7:0] ISP vertical output height
0x380C	HTS	0x04	RW	Bit[7:0]: HTS[15:8] Total horizontal timing size
0x380D	HTS	0x90	RW	Bit[7:0]: HTS[7:0] Total horizontal timing size
0x380E	VTS	0x0C	RW	Bit[6:0]: VTS[14:8] Total vertical timing size
0x380F	VTS	0x7C	RW	Bit[7:0]: VTS[7:0] Total vertical timing size
0x3810	ISP X WIN	0x00	RW	Bit[7:0]: isp_x_win[15:8] ISP horizontal windowing offset
0x3811	ISP X WIN	0x10	RW	Bit[7:0]: isp_x_win[7:0] ISP horizontal windowing offset
0x3812	ISP Y WIN	0x00	RW	Bit[7:0]: isp_y_win[15:8] ISP vertical windowing offset
0x3813	ISP Y WIN	0x08	RW	Bit[7:0]: isp_y_win[7:0] ISP vertical windowing offset
0x3814	X INC ODD	0x01	RW	Bit[4:0]: x_odd_inc
0x3815	X INC EVEN	0x01	RW	Bit[4:0]: x_even_inc
0x3816	Y_INC_ODD	0x01	RW	Bit[4:0]: y_odd_inc
0x3817	Y_INC_EVEN	0x01	RW	Bit[4:0]: y_even_inc

4.3 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration.

There are two main functions of the BLC:

- applying all normal pixel values based on the values of the black levels
- applying multiplication to all the pixel values based on digital gain

Black level adjustments can be made with registers 0x4004 and 0x4005.

table 4-3 BLC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4000	BLC_TOP_0	0xF8	RW	Bit[7]: off_trig_en Bit[6]: exp_chg_trig_en Bit[5]: gain_chg_trig_en Bit[4]: fmt_chg_trig_en Bit[3]: rst_trig_en Bit[2]: man_trig Bit[1]: off_frz_en Bit[0]: off_always_up
0x4004	BLC_TOP_4	0x00	RW	Bit[3:0]: blk_lvl_target_l[11:8]
0x4005	BLC_TOP_5	0x40	RW	Bit[7:0]: blk_lvl_target_l[7:0]
0x4011	BLC_TOP_11	0xFF	RW	Bit[5]: man_avg_en Bit[4]: off_chg_avg_en Bit[3]: fmt_chg_avg_en Bit[2]: gain_chg_avg_en Bit[1]: rst_avg_en Bit[0]: exp_chg_avg_en
0x4012	BLC_TOP_12	0x08	RW	Bit[7:0]: rst_trig_fn[7:0]
0x4013	BLC_TOP_13	0x02	RW	Bit[7:0]: fmt_manu_trig_fn[7:0]
0x4014	BLC_TOP_14	0x02	RW	Bit[7:0]: gain_exp_off_trig_fn[7:0]
0x4016	BLC_TOP_16	0x00	RW	Bit[3:0]: off_trig_th[11:8]
0x4017	BLC_TOP_17	0x04	RW	Bit[7:0]: off_trig_th[7:0]
0x4034	BLC_TOP_34	0x00	RW	Bit[1:0]: kcoef_b_man[9:8]
0x4035	BLC_TOP_35	0x80	RW	Bit[7:0]: kcoef_b_man[7:0]
0x4036	BLC_TOP_36	0x00	RW	Bit[1:0]: kcoef_gb_man[9:8]
0x4037	BLC_TOP_37	0x80	RW	Bit[7:0]: kcoef_gb_man[7:0]
0x4038	BLC_TOP_38	0x00	RW	Bit[1:0]: kcoef_gr_man[9:8]

table 4-3 BLC registers (sheet 2 of 2)

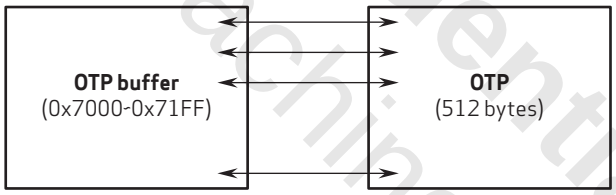
address	register name	default value	R/W	description
0x4039	BLC_TOP_39	0x80	RW	Bit[7:0]: kcoef_gr_man[7:0]
0x403A	BLC_TOP_3A	0x00	RW	Bit[1:0]: kcoef_r_man[9:8]
0x403B	BLC_TOP_3B	0x80	RW	Bit[7:0]: kcoef_r_man[7:0]

4.4 one-time programmable (OTP) memory

The OV13B10 supports a maximum of 512 bytes of one-time programmable (OTP) memory to store chip identification and manufacturing information, which can be used to update the sensor's default setting and can be controlled through the SCCB (see **table 4-4**). All 512 bytes are reserved for OmniVision.

There is a dedicated 512 byte buffer, which is used to temporarily store data to be programmed (written) into OTP or loaded (read) form OTP. The address for this OTP buffer ranges from 0x7000 to 0x71FF.

figure 4-3 OTP buffer



OTP loading data can be triggered at power up or by writing 0x01 to register 0x3D81. Power up loading data is enabled by register 0x3D85[3], and it is off by default. Auto mode and manual mode can be chosen by setting register 0x3D84[6] to 0 and 1, respectively, and by default, it is in auto mode. In auto mode, all data in the OTP will be loaded to the OTP buffer; while in manual mode, part of the data which is defined by the start address ({0x3D88, 0x3D89}) and the end address ({0x3D8A, 0x3D8B}) of the OTP will be loaded to the OTP buffer.

The OTP allocation is shown in **table 4-4**.

table 4-4 OTP allocation

start address	end address	bytes usage	assignment
0x7000	0x700F	16	production ID (reserved by OmniVision)
0x7010	0x71FF	496	reserved by OmniVision

The OTP memory access conditions are based on typical conditions: sensor wakeup, 2.8V AVDD, 1.2V DVDD, and 112 MHz system clock.

4.4.1 OTP write

This procedure is used to write specific bytes into the OTP. It is recommended to use this procedure to write to the OTP.

1. Set register 0x3D84[6] = 1 to enable manual mode for partial OTP access.
2. Set address range of OTP to be programmed:
   start address: {0x3D88, 0x3D89}
   end address: {0x3D8A, 0x3D8B}
3. Write data to buffer with address specified in step 2.
4. Set register 0x3D80[0] = 1 to program data stored in buffer into specified OTP bytes.

Example of partial OTP write:

```
6C 3D84 40; [6] partial mode enable
6C 3D85 00
6C 3D88 70; manual OTP start address for access, 0x7220 in this example
6C 3D89 20
6C 3D8A 70; manual OTP end address for access, 0x722F in this example
6C 3D8B 2F
6C 0100 01; stream mode enable
6C 7020 DD; Data[0]
6C 7021 A3; Data[1]
6C 7022 30; Data[2]
6C 7023 00; Data[3]
6C 7024 11; Data[4]
...
6C 702C 88; Data[12]
6C 702D 99; Data[13]
6C 702E AA; Data[14]
6C 702F BB; Data[15]
6C 3D80 01;[0] program enable
;delay 200ms
```

4.4.2 OTP read

This procedure is used to read specific bytes from OTP to buffer.

1. Set register 0x3D84[6] = 1 to enable manual mode for partial OTP access.
2. Set address range of OTP to be programmed:
   start address: {0x3D88, 0x3D89}
   end address: {0x3D8A, 0x3D8B}

3. Set register 0x3D81[0] = 1 to load data from specific OTP bytes to corresponding buffer.
4. User can read registers within range form start address to end address to check OTP data.

Example of OTP read (partial mode):

```
6C 3D84 40; [6] partial mode enable
6C 3D88 71; manual OTP start address for access
6C 3D89 00
6C 3D8A 71; manual OTP end address for access
6C 3D8B 0C
6C 3D81 01; OTP read enable
;only load data from OTP address 0x7100~0x710C
```

To use OTP memory under different operating conditions, please contact your local OmniVision FAE.

table 4-5 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x7000~ 0x71FF	OTP_SRAM	0x00	RW	Bit[7:0]: OTP buffer
0x3D80	OTP_PROGRAM_ CTRL	–	RW	Bit[7]: otp_pgenb_o 1: Program ongoing (read only) Bit[0]: OTP_program_enable Write 0 to 1 to start programming (write only)
0x3D81	OTP_LOA_CTRL	–	RW	Bit[7]: OTP_load_enable (read only) Bit[5]: OTP_bist_error (read only) Bit[4]: OTP_bist_done (read only) Bit[2]: bist_clr (write only) Bit[1]: autoload_m (write only) Bit[0]: OTP_rd 1: OTP load ongoing (read/write)
0x3D84	OTP_MODE_CTRL	0x00	RW	Bit[7]: Program disable 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode Bit[0]: bank_sram_switch

table 4-5 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D85	OTP_REG85	0x1B	RW	Bit[6]: r_otp_bist_comp_val Bit[5]: otp_bist_select 0: Compare with SRAM 1: Compare with zero Bit[4]: OTP_bist_enable Bit[3]: OTP power up load data enable Bit[2]: OTP wake up load setting enable Bit[1]: OTP hardware load setting enable Bit[0]: OTP software load setting enable
0x3D88	OTP_START_ ADDRESS	0x00	RW	Bit[7:0]: start_high_addr for manual mode
0x3D89	OTP_START_ ADDRESS	0x00	RW	Bit[7:0]: start_low_addr for manual mode
0x3D8A	OTP_EN_ADDRESS	0x03	RW	Bit[7:0]: end_high_addr for manual mode
0x3D8B	OTP_END_ADDRESS	0xFF	RW	Bit[7:0]: end_low_addr for manual mode
0x3D8C	OTP_SETTING_STT_ ADDRESS	0x00	RW	Bit[7:0]: start_high_addr for load setting
0x3D8D	OTP_SETTING_STT_ ADDRESS	0x00	RW	Bit[7:0]: start_low_addr for load setting
0x3D8E	OTP CHECK ERROR	–	R	Bit[7:0]: otp_check_err_addr[15:8]
0x3D8F	OTP CHECK ERROR	–	R	Bit[7:0]: otp_check_err_addr[7:0]

4.5 test pattern

table 4-6 test pattern registers

address	register name	default value	R/W	description
0x5080	ISP_CTRL_0	0x00	RW	Bit[7]: Test pattern enable 0: Disable 1: Enable Bit[6]: Rolling enable (rolling bar in test mode) 0: Disable 1: Enable Bit[5]: Transparent effect enable 0: Disable 1: Enable Bit[4]: Black/white or color square selection 0: Color 1: Black/white Bit[3:2]: Color bar style Bit[1:0]: Test mode select

figure 4-4 color bar types

color bar type 1
0x5080[3:2]=2'b00

color bar type 2
0x5080[3:2]=2'b01

color bar type 3
0x5080[3:2]=2'b10

color bar type 4
0x5080[3:2]=2'b11

5 image sensor processor digital functions

5.1 ISP block diagram

A simple ISP block diagram is shown in **figure 5-1** which includes some essential modules for RAW image process, such as OTP_DPC, DPC, etc.

figure 5-1 ISP block diagram

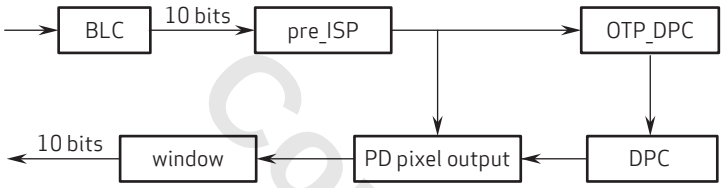


table 5-1 ISP top registers

address	register name	default value	R/W	description
0x5000	ISP_CTRL_0	0xED	RW	Bit[7]: WIN enable Bit[5]: DPC enable Bit[4]: OTP enable Bit[1]: PD bypass enable Bit[0]: ISP enable
0x5001	ISP_CTRL_1	0x07	RW	Bit[3]: Control signal latch mode Bit[1]: PD pix check enable Bit[0]: rst_protect_enable

5.2 defective pixel cancellation (DPC)

The main purpose of the DPC function is to remove white/black defect pixels. If the pixel is defective, DPC will use a value calculated from the neighboring normal pixels to replace it.

For DPC control, different types of clusters and correction criteria with gain change can be programmed by registers 0x5200 ~ 0x5210.

table 5-2 DPC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP_CTRL_0	0xED	RW	Bit[7]: WIN enable Bit[5]: DPC enable Bit[4]: OTP enable Bit[1]: PD bypass enable Bit[0]: ISP enable
0x5200	ISP_CTRL_0	0x1B	RW	Bit[7]: Enable tail Bit[6]: Enable tailing cluster Bit[5]: Enable 3x3 cluster Bit[4]: Enable saturate cross cluster Bit[3]: Enable cross cluster Bit[2]: Manual mode enable Bit[1]: Black pixel enable Bit[0]: White pixel enable
0x5201	ISP_CTRL_1	0x94	RW	Bit[7:6]: Vertical number list[2] Bit[5:4]: Vertical number list[1] Bit[3:2]: Vertical number list[0] Bit[1]: Enable G clip Bit[0]: Enable share buffer
0x5202	ISP_CTRL_2	0x2E	RW	Bit[5:4]: Bayer pattern order Bit[3:2]: Image boundary extend options Bit[1:0]: Vertical number list[3]
0x5203	ISP_CTRL_3	0x24	RW	Bit[6:3]: White pixel threshold list[0] Bit[2:0]: Maximum vertical number
0x5204	ISP_CTRL_4	0x12	RW	Bit[7:4]: White pixel threshold list[2] Bit[3:0]: White pixel threshold list[1]
0x5205	ISP_CTRL_5	0x41	RW	Bit[7:4]: Dark pixel threshold ratio Bit[3:0]: White pixel threshold list[3]
0x5206	ISP_CTRL_6	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: Cluster threshold
0x5207	ISP_CTRL_7	0x84	RW	Bit[7:4]: Pattern match threshold Bit[3:0]: Status threshold step
0x5208	ISP_CTRL_8	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold

table 5-2 DPC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5209	ISP_CTRL_9	0x00	RW	Bit[3:0]: Saturate pixel threshold for clusters
0x520A	ISP_CTRL_10	0x03	RW	Bit[4:0]: Gain threshold list[0]
0x520B	ISP_CTRL_11	0x0F	RW	Bit[4:0]: Gain threshold list[1]
0x520C	ISP_CTRL_12	0x1F	RW	Bit[4:0]: Gain threshold list[2]
0x520D	ISP_CTRL_13	0x0F	RW	Bit[7:0]: DPC level list[0]
0x520E	ISP_CTRL_14	0xFD	RW	Bit[7:0]: DPC level list[1]
0x520F	ISP_CTRL_15	0xF5	RW	Bit[7:0]: DPC level list[2]
0x5210	ISP_CTRL_16	0xF5	RW	Bit[7:0]: DPC level list[3]

5.3 window cut (WINC)

The main purpose of the WINC module is to make the image size to be real size by removing offset.

5.4 manual exposure compensation / manual gain compensation (MEC/MGC)

Manual exposure provides exposure time settings and sensor gain. The exposure values in registers 0x3500 ~ 0x3502 are in units of one line and must be applied by group function. Manual gain provides analog gain settings. The OV13B10 has a maximum 15.5x analog gain which is controlled by registers 0x3508 ~ 0x3509, where '0x0100' means 1x gain and '0x0F80' means 15.5x gain. Please contact your local OmniVision FAE for the gain lookup table.

note Maximum exposure = (VTS-8) lines, minimum exposure = 4 lines.

table 5-3 AEC_pk registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3500	AEC_PK_L_0	0x00	RW	Bit[7:0]: r_expo_coarse[23:16]
0x3501	AEC_PK_L_1	0x00	RW	Bit[7:0]: r_expo_coarse[15:8]
0x3502	AEC_PK_L_2	0x40	RW	Bit[7:0]: r_expo_coarse[7:0]

table 5-3 AEC_pk registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3503	AEC_CFG_L_3	0xA8	RW	Bit[7]: Real gain 0: real_gain auto 1: real_gain manual Bit[6]: dig_gain_delay option 0: Digital gain (ISP use) has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Digital gain (ISP use) has no delay on gain control, takes effect immediately in next frame Bit[5]: format_change_update_en Bit[4]: gain_delay option 0: Sensor/gain has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Sensor/gain has no delay on gain control, takes effect immediately in next frame Bit[3]: AEC enable 0: Auto AEC enable 1: Manual AEC enable
0x3508	AEC_PK_L_8	0x01	RW	Bit[3:0]: r_real_gain[10:7] gain_coarse
0x3509	AEC_PK_L_9	0x00	RW	Bit[7:1]: r_real_gain[6:0] gain_fine
0x350A	AEC_CFG_L_10	0x01	RW	Bit[1:0]: dig_gain_coarse_b
0x350B	AEC_CFG_L_11	0x00	RW	Bit[7:0]: dig_gain_fine_b[9:2] for global digital gain
0x350C	AEC_CFG_L_12	0x00	RW	Bit[7:6]: dig_gain_fine_b[1:0] for global digital gain

table 5-3 AEC_pk registers (sheet 3 of 3)

address	register name	default value	R/W	description

0x350D	AEC_CFG_L_13	0x00	RW	Bit[1:0]: snr_gain_map[1:0]
				00: Default
				cmp_gain[2:0] = snr_gain_coarse[2:0];
				dac_gain[1:0] = snr_gain_coarse[4:3];
				01: Opt1
				cmp_gain[2:0] ={snr_gain_coarse[3:2], snr_gain_coarse[0]};
				dac_gain[1:0] ={snr_gain_coarse[4], snr_gain_coarse[1]};
				10: Opt2
				cmp_gain[2:0] ={snr_gain_coarse[3], snr_gain_coarse[1:0]};
				dac_gain[1:0] ={snr_gain_coarse[4], snr_gain_coarse[2]};
				11: Opt3
				cmp_gain[2:0] = snr_gain_coarse[3:1];
				Dac_gain[1:0] = {snr_gain_coarse[4], snr_gain_coarse[0]}

5.5 digital gain

Manual digital gain provides the same gain for R, G, and B channels. The OV13B10 supports up to 4x digital gain.

table 5-4 digital gain registers

address	register name	default value	R/W	description
0x3503	AEC_CFG_L_3	0xA8	RW	Bit[7]: Real gain 0: real_gain auto 1: real_gain manual Bit[6]: dig_gain_delay option 0: Digital gain (ISP use) has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Digital gain (ISP use) has no delay on gain control, takes effect immediately in next frame Bit[5]: format_change_update_en Bit[4]: gain_delay option 0: Sensor/gain has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Sensor/gain has no delay on gain control, takes effect immediately in next frame Bit[3]: AEC enable 0: Auto AEC enable 1: Manual AEC enable
0x350A	AEC_CFG_L_10	0x01	RW	Bit[1:0]: dig_gain_coarse_b
0x350B	AEC_CFG_L_11	0x00	RW	Bit[7:0]: dig_gain_fine_b[9:2] for global digital gain
0x350C	AEC_CFG_L_12	0x00	RW	Bit[7:6]: dig_gain_fine_b[1:0] for global digital gain

6 register tables

The following tables provide descriptions of the device control registers contained in the OV13B10. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read when SID=0 (when SID=1, 0x20 for write and 0x21 for read).

6.1 PLL [0x0300 - 0x0306, 0x0320 - 0x0329, 0x3020, 0x3106]

table 6-1 PLL registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x0300	PLL_CTRL_0	0x00	RW	Bit[7:3]: Not used Bit[2]: pll1_rst Bit[1]: Not used Bit[0]: pll1_bypass
0x0301	PLL_CTRL_1	0x80	RW	Bit[7]: pll1_pix_bitdiv 0: /4 1: /5 Bit[6]: pll1_predivp 0: /1 1: /2 Bit[5:4]: Not used Bit[3]: pll1_sys_bitdiv 0: /4 1: /5 Bit[2:0]: Not used
0x0302	PLL_CTRL_2	0x01	RW	Bit[7:6]: Not used Bit[5]: pll1_div_rst_sync_en Bit[4:3]: Not used Bit[2:0]: pll1_cp
0x0303	PLL_CTRL_3	0x01	RW	Bit[7:3]: Not used Bit[2:0]: pll1_prediv 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0304	PLL_CTRL_4	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll1_multiplier[9:8]
0x0305	PLL_CTRL_5	0x46	RW	Bit[7:0]: pll1_multiplier[7:0]

table 6-1 PLL registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x0306	PLL_CTRL_6	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll1_divpix 00: /1 01: /2 10: /3 11: /4
0x0320	PLL_CTRL_20	0x00	RW	Bit[7:3]: Not used Bit[2]: pll2_rst Bit[1]: r_pll2_div_rst_sync_en Bit[0]: r_pll2_bypass
0x0321	PLL_CTRL_21	0x01	RW	Bit[7:3]: Not used Bit[2:0]: pll2_cp
0x0322	RSVD	–	–	Reserved
0x0323	PLL_CTRL_23	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pll2_prediv 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0324	PLL_CTRL_24	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll2_multiplier[9:8]
0x0325	PLL_CTRL_25	0x38	RW	Bit[7:0]: pll2_multiplier[7:0]
0x0326	PLL_CTRL_26	0x01	RW	Bit[7]: pll2_predivp 0: /1 1: /2 Bit[6:2]: Not used Bit[1:0]: pll2_divsa1 00: /5 01: /6 10: /7 11: /8
0x0327	PLL_CTRL_27	0x05	RW	Bit[7:3]: Not used Bit[2:0]: pll2_divsram Control bit value = bit[2:0] + 1
0x0328	RSVD	–	–	Reserved

table 6-1 PLL registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x0329	PLL_CTRL_29	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pll2_divdac 00: /1 01: /2 10: /3 11: /4
0x3020	CLOCK SEL	0x9B	RW	Bit[7:4]: Not used Bit[3]: pclk_sel 0: /1 1: /2 Bit[2:0]: Not used
0x3106	SRB HOST INPUT DIS	0x15	RW	Bit[7:4]: Not used Bit[3:2]: sys_clk_div 00: /1 01: /2 10: /4 11: /8 Bit[1:0]: Not used

6.2 system [0x0100 - 0x0103, 0x3002 - 0x3008, 0x300A - 0x3022, 0x302A]

table 6-2 system registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x0100	MODEL_SELECT	0x00	RW	Bit[7:1]: Not used Bit[0]: Mode select 0: software_standby 1: Streaming
0x0101~ 0x0102	NOT USED	–	–	Not Used
0x0103	SOFTWARE_RST	–	W	Bit[7:1]: Not used Bit[0]: software_reset
0x3002	PAD OEN2	0x21	RW	Bit[7]: io_fsin_oen Bit[6]: io_vsync_oen Bit[5:0]: Reserved
0x3003	SCCB_ID	0x6C	RW	Bit[7:0]: SCCB programmable ID
0x3004	SCCB ID	0x20	RW	Bit[7:0]: sccb_id SCCB backup programmed ID
0x3005	SCCB_ID_2	0x42	RW	Bit[7:0]: sccb_id2

table 6-2 system registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x3006~ 0x3007	NOT USED	–	–	Not Used
0x3008	PAD_OUT2	0x00	RW	Bit[7]: io_fsin_o Bit[6]: io_vsync_o Bit[5:3]: Reserved Bit[2]: io_sda_o Bit[1:0]: Reserved
0x300A	CHIP ID	0x56	R	Bit[7:0]: chip_id[23:16]
0x300B	CHIP ID	0x0D	R	Bit[7:0]: chip_id[15:8]
0x300C	CHIP ID	0x42	R	Bit[7:0]: chip_id[7:0]
0x300D~ 0x300F	NOT USED	–	–	Not Used
0x3010	PAD SEL2	0x00	RW	Bit[7]: io_fsin_sel Bit[6]: io_vsync_sel Bit[5:3]: Reserved Bit[2]: io_sda_sel Bit[1:0]: Reserved

table 6-2 system registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x3011	WAKE_UP_DELAY	0x4C	RW	Bit[7]: Not used Bit[6:4]: Digital stream on delay 000: Delay 2^8 pad clock cycle after stream 001: Delay 2^9 pad clock cycle after stream 010: Delay 2^10 pad clock cycle after stream 011: Delay 2^11 pad clock cycle after stream 100: Delay 2^12 pad clock cycle after stream 101: Delay 2^13 pad clock cycle after stream 110: Delay 2^14 pad clock cycle after stream 111: Delay 2^15 pad clock cycle after stream Bit[3]: Not used Bit[2:0]: Analog stream on delay 000: Delay 2^9 pad clock cycle after stream 001: Delay 2^10 pad clock cycle after stream 010: Delay 2^11 pad clock cycle after stream 011: Delay 2^12 pad clock cycle after stream 100: Delay 2^13 pad clock cycle after stream 101: Delay 2^14 pad clock cycle after stream 110: Delay 2^15 pad clock cycle after stream 111: Delay 2^16 pad clock cycle after stream
0x3012	CLK_GATE_MASK	0x00	RW	Bit[7]: Not used Bit[6]: pclk_mipi_clk_gate_mask Bit[5:0]: Not used

table 6-2 system registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x3013	CLK_GATE_MASK	0x00	RW	Bit[7]: sclk_dpcm_clk_gate_mask Bit[6]: sclk_mipi_clk_gate_mask Bit[5]: sclk_tpm sclk_clip_clk_gate_mask Bit[4]: Not used Bit[3]: sclk_isp sclk_isp_fc_clk_gate_mask Bit[2]: sclk_blc_clk_gate_mask Bit[1]: sclk_sync_fifo srmclk_sync_fifo_clk_gate_mask Bit[0]: srmclk_psram_clk_gate_mask
0x3014	FREX_RST_MASK	0x08	RW	Bit[7]: aec_frex_rst_mask Bit[6]: BLC/ISP/sync_fifo FREX reset mask Bit[5:4]: Not used Bit[3]: mipi_frex_rst_mask Bit[2]: vfifo_frex_rst_mask Bit[1]: tmp_frex_rst_mask Bit[0]: mipi_phy_frex_rst_mask
0x3015	PUMP CLK DIV	0x10	RW	Bit[7]: Not used Bit[6:4]: Npump clock divider 000: /2 001: /4 010: /8 011: /16 100: /32 Others: Disable pump_clk Bit[3]: pd_mipi_auto mode 0: Use original reset as pd_mipi_auto 1: Use synchronous reset as pd_mipi_auto Bit[2:0]: Ppump clock divider 000: /2 001: /4 010: /8 011: /16 100: /32 Others: Disable pump_clk

table 6-2 system registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x3016	MIPI SC CTRL	0x72	RW	Bit[7:5]: mipi_lane_mode N+1 lane Bit[4]: mipi_en 0: MIPI disable 1: MIPI enable Bit[3:2]: r_phy_pd_mipi Bit[1]: phy_rst option 0: rst_sync cannot reset PHY 1: Reset PHY when rst_sync Bit[0]: lane_dis option 0: Not used 1: Disable lanes when pd_mipi
0x3017	MIPI SC CTRL	0x00	RW	Bit[7:4]: Not used Bit[3:0]: MIPI lane disable
0x3018	CLK_CTRL	0xF0	RW	Bit[7]: tclk_tc enable Bit[6]: tclk_snr_ctrl enable Bit[5]: srmclk_psram enable Bit[4]: srmclk_syncfifo enable Bit[3]: rst_tc Bit[2]: rst_snr_ctrl and psram_ctrl Bit[1]: Not used Bit[0]: rst_syncfifo
0x3019	CTRL_R19	0xF0	RW	Bit[7:6]: Not used Bit[5]: tclk_psv_ctrl Bit[4:2]: Reserved Bit[1]: rst_psv Bit[0]: Reserved
0x301A	CLKRST0	0xF0	RW	Bit[7:4]: Reserved Bit[3]: mipi_phy_rst_o Bit[2:0]: Reserved
0x301B	CLKRST1	0xD0	RW	Bit[7]: sclk_blc enable Bit[6]: sclk_isp enable Bit[5:4]: Reserved Bit[3]: rst_blc Bit[2]: rst_isp Bit[1:0]: Reserved
0x301C	CLKRST2	0xF0	RW	Bit[7]: Reserved Bit[6]: sclk_mipi_en Bit[5]: Reserved Bit[4]: sclk_efuse_en Bit[3]: Reserved Bit[2]: rst_mipi Bit[1]: Reserved Bit[0]: rst_efuse

table 6-2 system registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x301D	CLKRST3	0xD8	RW	Bit[7]: sclk_asram_tst_en Bit[6]: sclk_grp_en Bit[5]: sclk_bist_en Bit[4]: sclk_aec_en Bit[3]: rst_asram_tst Bit[2]: rst_grp Bit[1]: rst_bist Bit[0]: rst_aec
0x301E	CLKRST4	0xF0	RW	Bit[7:5]: Reserved Bit[4]: pclk_mipi_en Bit[3:0]: Reserved
0x301F	CLKRST5	0xD0	RW	Bit[7]: Reserved Bit[6]: sclk_isp_fc_en Bit[5]: sclk_dpcm_en Bit[4]: sclk_clip_en Bit[3]: Reserved Bit[2]: rst_isp_fc Bit[1]: rst_dpcm Bit[0]: rst_clip
0x3020	CLOCK SEL	0x9B	RW	Bit[7:5]: Not used Bit[4]: sccb_id2_nack 0: SCCB slave returns normal ACK 1: SCCB slave does not return ACK Bit[3]: PCLK_div 0: /1 (choose pll_pclk_i) 1: /2 (choose pll_pclk_d2) Bit[2]: Not used Bit[1]: pclk_inv Reverse PCLK Bit[0]: sclk2x_sel 0: Choose pll_sclk_i 1: Choose_pll_sclk_d2

table 6-2 system registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x3021	MISC CTRL	0x23	RW	Bit[7]: Not used Bit[6]: Sleep no latch option 0: Sensor enters into sleep mode in blanking period defined by bit[5] 1: Sensor enters into sleep mode immediately Bit[5]: fst_stby_ctr Works only when bit[6] = 0 0: Software standby enters at vertical blanking 1: Software standby enters at line blanking Bit[4]: mipi_ctr_en 0: Disable function 1: Enable MIPI remote reset and suspend control SC Bit[3]: mipi_rst_sel 0: MIPI remote resets all registers 1: MIPI remote resets all digital modules Bit[2]: gpio_pclk_en Bit[1]: frex_ef_sel Bit[0]: cen_global_o
0x3022	MIPI SC CTRL	0x01	RW	Bit[7:4]: mipi_bit_sel 0100: 8-bit mode 0101: 10-bit mode 0110: 12-bit mode 1000: 16-bit mode Others: 10-bit mode Bit[3]: Reserved Bit[2]: Clock lane disable 1 Bit[1]: Clock lane disable 0 Bit[0]: pd_mipi_by software reset enable
0x302A	SUB ID	–	R	Bit[7:4]: Process Bit[3:0]: Version

6.3 SCCB [0x3100 - 0x3103, 0x3106 - 0x3109]

table 6-3 SCCB registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3100	SCCB CTRL	0x00	RW	Bit[7:4]: Not used Bit[3]: r_sda_dly_en Bit[2:0]: r_sda_dly
0x3101	SCCB OPT	0x12	RW	Bit[7:5]: Not used Bit[4]: en_ss_addr_inc Bit[3]: r_sda_byp_sync 0: Two clock stage sync for sda_i 1: No sync for sda_i Bit[2]: r_scl_byp_sync 0: Two clock stage sync for scl_i 1: No sync for scl_i Bit[1]: r_msk_glitch Bit[0]: r_msk_stop
0x3102	SCCB FILTER	0x01	RW	Bit[7:4]: Not used Bit[3]: r_scl_chk_en Bit[2:0]: r_scl_pulse_num_min
0x3103	PLL_CLK_SEL	0x1F	RW	Bit[7:5]: Not used Bit[4]: arb_sleep_en Bit[3]: r_grp_sleep_rst_en Bit[2]: r_arb_sleep_rst_en Bit[1]: r_sclk_grp_sw_sft_stb_dis Bit[0]: grp_sclk_sel
0x3106	SRB HOST INPUT DIS	0x25	RW	Bit[7]: sramclk_cutoff_byp Bit[6]: sa1clk_cutoff_byp Bit[5]: ppump_clk_all_on Bit[4]: ppump_clk_sw Bit[3:2]: sclk_sel Bit[1]: rst_arb Bit[0]: arb_clk_en
0x3107	SRB_CTRL	0x81	RW	Bit[7]: npump_clk_all_on Bit[6]: npump_clk_sw Bit[5]: auto_sleep_en Bit[4]: pd_mipi_dis_aslp Bit[3]: pumpclk_cutoff_byp Bit[2]: pclk_cutoff_byp Bit[1]: sclk_cutoff_byp Bit[0]: sclk_inv

table 6-3 SCCB registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3108	SRB_CTRL	0xFD	RW	Bit[7]: srclk_all_on Bit[6]: npump2_lp_pd_dis Bit[5]: npump2_pd_dis Bit[4]: npump1_pd_dis Bit[3]: ppump_lp_pd_dis Bit[2]: ppump_pd_dis Bit[1]: pll_sclk_selection 0: pll_sclk_i 1: p_clk_i Bit[0]: Sleep control
0x3109	SRB_CTRL	0x03	RW	Bit[7:2]: Not used Bit[1]: pclk_all_on Bit[0]: sclk_all_on

6.4 group hold [0x3200 - 0x320F]

table 6-4 group hold registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM Actual address is {0x3200[5:0], 4'h0}
0x3201	GROUP ADR1	0x08	RW	Group1 Start Address in SRAM Actual address is {0x3201[5:0], 4'h0}
0x3202	GROUP ADR2	0x10	RW	Group2 Start Address in SRAM Actual address is {0x3202[5:0], 4'h0}
0x3203	GROUP ADR3	0x18	RW	Group3 Start Address in SRAM Actual address is {0x3203[5:0], 4'h0}
0x3204	GROUP LEN0	–	R	Length of Group0
0x3205	GROUP LEN1	–	R	Length of Group1
0x3206	GROUP LEN2	–	R	Length of Group2
0x3207	GROUP LEN3	–	R	Length of Group3

table 6-4 group hold registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch 1110: Fast group launch Others: Reserved Bit[3:0]: Group ID 0000: Group bank 0 0001: Group bank 1 1010: Group bank 2 1110: Group bank 3 Others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	When register 0x320B[7] = 1 Bit[7]: Not used Bit[6:5]: Group number that group will switch back to after launch group 0 in auto switch mode Bit[4:0]: grp0_frms Number of frames stay in group 0 before auto switch to group defined by 0x3209[6:5] When register 0x320B[2] = 1 Bit[7:0]: Number of frames stay in group 0 before auto switch to group defined by 0x320B[1:0]
0x320A	GRP1_PERIOD	0x00	RW	Bit[7:0]: Number of frames stay in second group in context switch mode defined by 0x320B[1:0] Works only when 0x320B[2] = 1)
0x320B	GRP_SWCTRL	0x11	RW	Bit[7]: auto_sw Auto launch mode enable Bit[6:5]: Not used Bit[4]: frame_cnt_trig 0: EOF as frame count trigger 1: Group write as frame count trigger Bit[3]: group_switch_repeat Bit[2]: context_en Contact switch mode enable Bit[1:0]: Second group selection
0x320C	SRAM TEST	0x02	R/W	Bit[7:6]: Not used Bit[5]: sram_RME Bit[4]: Group hold SRAM test enable Bit[3:0]: Group hold SRAM RM[3:0]

table 6-4 group hold registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x320D	GRP_ACT	–	R	Bit[7:4]: Not used Bit[3:0]: grp_act Indicates which group is active
0x320E	FRAME_CNT_GRP0	–	R	Bit[7:0]: frame_cnt_grp0
0x320F	FRAME_CNT_GRP1	–	R	Bit[7:0]: frame_cnt_grp1

6.5 AEC_pk [0x3500 - 0x350D, 0x351C - 0x352D]

table 6-5 AEC_pk registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3500	AEC_PK_L_0	0x00	RW	Bit[7:0]: r_expo_coarse[23:16]
0x3501	AEC_PK_L_1	0x00	RW	Bit[7:0]: r_expo_coarse[15:8]
0x3502	AEC_PK_L_2	0x40	RW	Bit[7:0]: r_expo_coarse[7:0]
0x3503	AEC_CFG_L_3	0xA8	RW	Bit[7]: Real gain 0: real_gain auto 1: real_gain manual Bit[6]: dig_gain_delay option 0: Digital gain (ISP use) has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Digital gain (ISP use) has no delay on gain control, takes effect immediately in next frame Bit[5]: format_change_update_en Bit[4]: gain_delay option 0: Sensor/gain has 1 frame delay latch, takes effect in second occurring frame and will sync with exposure 1: Sensor/gain has no delay on gain control, takes effect immediately in next frame Bit[3]: AEC enable 0: Auto AEC enable 1: Manual AEC enable Bit[2:0]: Reserved

table 6-5 AEC_pk registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3504	AEC_CFG_L_4	0x08	RW	Bit[7]: real_gain_as_snr_gain Bit[6]: isp_real_gain_blc Bit[5]: Reserved Bit[4]: gain_delay_by_expo_change Bit[3]: initial_update_en Bit[2]: Use B channel digital gain apply to all channels Bit[1]: vdl_sync_en Bit[0]: Not used
0x3505	AEC_PK_L_5	0x00	RW	Bit[7:1]: Not used Bit[0]: manual_update_en[0]
0x3506	AEC_PK_FINE_EXP_L_6	0x00	RW	Bit[7:0]: expo_fine[15:8]
0x3507	AEC_PK_FINE_EXP_L_7	0x00	RW	Bit[7:0]: expo_fine[7:0]
0x3508	AEC_PK_L_8	0x01	RW	Bit[7:4]: Not used Bit[3:0]: r_real_gain[10:7] gain_coarse
0x3509	AEC_PK_L_9	0x00	RW	Bit[7:1]: r_real_gain[6:0] gain_fine Bit[0]: Not used
0x350A	AEC_CFG_L_10	0x01	RW	Bit[7:2]: Not used Bit[1:0]: dig_gain_coarse_b
0x350B	AEC_CFG_L_11	0x00	RW	Bit[7:0]: dig_gain_fine_b[9:2] for global digital gain
0x350C	AEC_CFG_L_12	0x00	RW	Bit[7:6]: dig_gain_fine_b[1:0] for global digital gain Bit[5:0]: Not used

table 6-5 AEC_pk registers (sheet 3 of 4)

address	register name	default value	R/W	description

0x350D	AEC_CFG_L_13	0x00	RW	Bit[7:2]: Not used
				Bit[1:0]: snr_gain_map[1:0]
				00: Default
				cmp_gain[2:0] = snr_gain_coarse[2:0];
				dac_gain[1:0] = snr_gain_coarse[4:3];
				01: Opt1
				cmp_gain[2:0] ={snr_gain_coarse[3:2], snr_gain_coarse[0]};
				dac_gain[1:0] ={snr_gain_coarse[4], snr_gain_coarse[1]};
				10: Opt2
				cmp_gain[2:0] ={snr_gain_coarse[3], snr_gain_coarse[1:0]};
				dac_gain[1:0] ={snr_gain_coarse[4], snr_gain_coarse[2]};
				11: Opt3
				cmp_gain[2:0] = snr_gain_coarse[3:1];
				dac_gain[1:0] = {snr_gain_coarse[4], snr_gain_coarse[0]}

0x351C	AEC_CFG_L_28	–	R	Bit[7:0]: expo_coarse_cur[15:8]
0x351D	AEC_CFG_L_29	–	R	Bit[7:0]: expo_coarse_cur[7:0]
0x351E	AEC_CFG_L_30	–	R	Bit[7]: Not used Bit[6:0]: gain_coarse_cur_use[6:0]
0x351F	AEC_CFG_L_31	–	R	Bit[7:1]: gain_fine_cur_use[6:0] Bit[0]: Not used
0x3520	AEC_CFG_L_32	–	R	Bit[7]: Not used Bit[6:0]: gain_coarse_cur_org[6:0]
0x3521	AEC_CFG_L_33	–	R	Bit[7:1]: gain_fine_cur_org[6:0] Bit[0]: Not used
0x3522	AEC_CFG_L_34	–	R	Bit[7]: Not used Bit[6:0]: snr_gain_coarse_cur[6:0]
0x3523	AEC_CFG_L_35	–	R	Bit[7:1]: snr_gain_fine_cur[6:0] Bit[0]: Not used
0x3524	AEC_CFG_L_36	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_b[3:0]

table 6-5 AEC_pk registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3525	AEC_CFG_L_37	–	R	Bit[7:0]: cur_dig_gain_fine_b[9:2]
0x3526	AEC_CFG_L_38	–	R	Bit[7:6]: cur_dig_gain_fine_b[1:0] Bit[5:0]: Not used
0x3527	AEC_CFG_L_39	–	R	Bit[7]: Not used Bit[6:0]: real_gain_blc_coarse[6:0]
0x3528	AEC_CFG_L_40	–	R	Bit[7:4]: real_gain_blc_fine[3:0] Bit[3:0]: Not used
0x3529	AEC_CFG_L_41	–	R	Bit[7:3]: Not used Bit[2:0]: real_gain_isp_coarse[10:8]
0x352A	AEC_CFG_L_42	–	R	Bit[7:0]: real_gain_isp_coarse[7:0]
0x352B	AEC_CFG_L_43	–	R	Bit[7:4]: real_gain_isp_fine[3:0] Bit[3:0]: Not used
0x352C	AEC_PK_FINE_EXP_L_44	–	R	Bit[7:0]: expo_fine_cur[15:8]
0x352D	AEC_PK_FINE_EXP_L_45	–	R	Bit[7:0]: expo_fine_cur[7:0]

6.6 ANA [0x3600 - 0x3629, 0x3660 - 0x367F, 0x3681 - 0x3684, 0x36F0 - 0x36F2]

table 6-6 ANA registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3600~ 0x3629	ANALOG CONTROL	–	–	Analog Control
0x3660	CORE TOP REG00	0x00	RW	Bit[7]: asram_clk_sel Selection clock for analog SRAM test 0: Choose daclk (default 648MHz) 1: Choose pll2_sclk (default 216MHz) Bit[6]: r_rst_otp_sleep_dis 0: Allow software reset to reset OTP 1: Disable software reset to reset OTP Bit[5]: r_rst_ana_sleep_dis 0: Allow software reset to reset analog circuit 1: Disable software reset to reset analog circuit Bit[4]: pll1_sysclk_sel 0: SCLK comes from PLL1 1: SCLK comes from PLL2 Bit[3]: r_fmt_eof_sel 0: Format EOF input comes from ISPFC EOF 1: Format EOF input comes from mipi_eof Bit[2]: rip_sof_en 0: MIPI SOF input comes from timing control SOF (original SOF) 1: MIPI SOF input comes from ISPFC SOF (after ripple delay) Bit[1]: pll_sysclk_sel PLL2 SCLK is used as TCLK after a series of mux 0: pll2_sclk_real comes from pll2_mux_sclk 1: pll2_sclk_real comes from pll2_daclk Bit[0]: mipi_sel_aslp_dis 0: Allow MIPI clock to enter into low power mode 1: Disable MIPI clock to enter into low power mode

table 6-6 ANA registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3661	CORE TOP REG01	0x80	RW	Bit[7]: r_sa1clk_sel 0: pll_sa1_clk comes from sa1_clk_d24 (divided pll1_sclk) 1: pll_sa1_clk comes from pll1_sclk Bit[6:4]: r_bit_shift_mode Shift left ISP output data certain bits 000: No shift 001: Shift left 1 bit 010: Shift left 2 bits 011: Shift left 3 bits Others: Left shift 4 bits Bit[3]: byp_isp 0: No bypass, normal data path 1: Bypass ISP data, HREF, valid; these components all come from sync FIFO Bit[2]: r_bit_shift_clip_en 0: No clip, add zero at low bits 1: Clip all to one when one is shift out Bit[1]: r_pump_clk_sel 0: pll_pump_clk comes from pll2_sclk 1: pll_pump_clk comes from pll1_sclk Bit[0]: pll2_sysclk_sel 0: pll2_mux_sclk comes from pll2_sclk 1: pll2_mux_sclk comes from pll1_sclk
0x3662	CORE TOP REG02	0x90	RW	Bit[7]: Not used Bit[6:0]: r_blc_black_num BLC black line number used for BLC
0x3663	CORE TOP REG03	0x26	RW	Bit[7]: Reserved Bit[6:5]: I/O pad drive capability 00: 1x 01: 2x 10: 3x 11: 4x Bit[4:3]: Not used Bit[2]: FSIN selection 0: P_FSIN comes from input 1: P_FSIN fixed at 0 Bit[1]: VSYNC selection 0: P_VSYNC comes from input 1: P_VSYNC fixed at 0 Bit[0]: Not used

table 6-6 ANA registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3664	CORE TOP REG04	0x71	RW	Bit[7:4]: Reserved Bit[3]: sramclk_sel 0: pll2_sram_clk_real comes from pll2_sram_clk2x 1: pll2_sram_clk_real comes from pll1_sram_clk1x Bit[2:0]: Reserved
0x3665	CORE TOP REG05	0x07	RW	Bit[7:4]: Reserved Bit[3]: sa1clk_d24_sel 0: sa1_clk_d24 as sa1_clk_d2 1: sa1_clk_d24 as sa1_clk_d4 Bit[2:0]: Reserved
0x3666~ 0x36F2	CORE TOP CONTROL	–	–	Core Top Control

6.7 sensor top [0x3700 - 0x37FF]

table 6-7 sensor top control registers

address	register name	default value	R/W	description
0x3700~ 0x37FF	SENSOR TOP CONTROL	–	–	Sensor Top Control

6.8 timing control [0x3800 - 0x3835]

table 6-8 timing control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x3800	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[15:8] Array horizontal start point
0x3801	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point
0x3802	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[15:8] Array vertical start point

table 6-8 timing control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x3803	Y ADDR START	0x08	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point
0x3804	X ADDR END	0x10	RW	Bit[7:0]: x_addr_end[15:8] Array horizontal end point
0x3805	X ADDR END	0x8F	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point
0x3806	Y ADDR END	0x0C	RW	Bit[7:0]: y_addr_end[15:8] Array vertical end point
0x3807	Y ADDR END	0x47	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point
0x3808	X OUTPUT SIZE	0x10	RW	Bit[7:0]: x_output_size[15:8] ISP horizontal output width
0x3809	X OUTPUT SIZE	0x70	RW	Bit[7:0]: x_output_size[7:0] ISP horizontal output width
0x380A	Y OUTPUT SIZE	0x0C	RW	Bit[7:0]: y_output_size[15:8] ISP vertical output height
0x380B	Y OUTPUT SIZE	0x30	RW	Bit[7:0]: y_output_size[7:0] ISP vertical output height
0x380C	HTS	0x04	RW	Bit[7:0]: HTS[15:8] Total horizontal timing size
0x380D	HTS	0x90	RW	Bit[7:0]: HTS[7:0] Total horizontal timing size
0x380E	VTS	0x0C	RW	Bit[7]: Reserved Bit[6:0]: VTS[14:8] Total vertical timing size
0x380F	VTS	0x7C	RW	Bit[7:0]: VTS[7:0] Total vertical timing size
0x3810	ISP X WIN	0x00	RW	Bit[7:0]: isp_x_win[15:8] ISP horizontal windowing offset
0x3811	ISP X WIN	0x10	RW	Bit[7:0]: isp_x_win[7:0] ISP horizontal windowing offset
0x3812	ISP Y WIN	0x00	RW	Bit[7:0]: isp_y_win[15:8] ISP vertical windowing offset
0x3813	ISP Y WIN	0x08	RW	Bit[7:0]: isp_y_win[7:0] ISP vertical windowing offset
0x3814	X INC ODD	0x01	RW	Bit[7:5]: Not used Bit[4:0]: x_odd_inc

table 6-8 timing control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x3815	X INC EVEN	0x01	RW	Bit[7:5]: Not used Bit[4:0]: x_even_inc
0x3816	Y_INC_ODD	0x01	RW	Bit[7:5]: Not used Bit[4:0]: y_odd_inc
0x3817	Y_INC_EVEN	0x01	RW	Bit[7:5]: Not used Bit[4:0]: y_even_inc
0x3818	VSYNC START	0x00	RW	Bit[7:0]: vsync_start[15:8] VSYNC start point
0x3819	VSYNC START	0x00	RW	Bit[7:0]: vsync_start[7:0] VSYNC start point
0x381A	VSYNC END	0x00	RW	Bit[7:0]: vsync_end[15:8] VSYNC end point
0x381B	VSYNC END	0x01	RW	Bit[7:0]: vsync_end[7:0] VSYNC end point
0x381C	BLC_NUM_OPTION	0x18	RW	Bit[7:5]: ablc_adj Bit[4:0]: ablc_use_num
0x381D	BLC_NUM_OPTION	0x00	RW	Bit[7:6]: Not used Bit[5]: r_man_blc_num_sel Bit[4:0]: r_man_blc_num
0x381E	BLC_NUM_OPTION	0x20	RW	Bit[7]: Not used Bit[6:0]: r_ablc_num
0x381F	VTS_EXP_DIFF	0x10	RW	Bit[7:5]: Not used Bit[4:0]: vts_exp_difference
0x3820	FORMAT1	0x80	RW	Bit[7:6]: Not used Bit[5]: Black line vertical flip control 0: Normal 1: Vertical flip Bit[4]: Image vertical flip enable 0: Normal 1: Vertical flip Bit[3]: Image horizontal mirror disable 0: Image horizontal mirror enable 1: Normal Bit[2]: hbin4_o Bit[1]: hbin2_o Bit[0]: vbinf_o

table 6-8 timing control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x3821	FORMAT2	0x30	RW	Bit[7:6]: Not used Bit[5]: r_y_auto_cut_en Bit[4]: r_x_auto_cut_en Bit[3:2]: Not used Bit[1]: Reserved Bit[0]: vsub48_blc
0x3822	REG22	0x04	RW	Bit[7]: r_max_exp_sel Bit[6]: r_vts_dly_2frame Bit[5]: r_fix_cnt_en Bit[4]: vts_add_dis Bit[3:0]: r_grp_adj
0x3823	REG23	0x08	RW	Bit[7]: ext_vs_re Bit[6]: ext_vs_en Bit[5]: vts_no_latch Bit[4]: init_man Bit[3:0]: r_ext_vsync_div
0x3824	CS RST FSIN	0x00	RW	Bit[7:0]: cs_rst_fsin[15:8] CS reset value at vs_ext
0x3825	CS RST FSIN	0x20	RW	Bit[7:0]: cs_rst_fsin[7:0] CS reset value at vs_ext
0x3826	R RST FSIN	0x00	RW	Bit[7:0]: r_rst_fsin[15:8] R reset value at vs_ext
0x3827	R RST FSIN	0x08	RW	Bit[7:0]: r_rst_fsin[7:0] R reset value at vs_ext
0x3828	RSVD	–	–	Reserved
0x3829	VTS ADJUST	0x08	RW	Bit[7:6]: Not used Bit[5:4]: vts_adj_threshold Bit[3:0]: tc_r initial threshold
0x382A	VTS ADJUST	0x00	RW	Bit[7:0]: man_vts_adj_val[15:8]
0x382B	VTS ADJUST	0x08	RW	Bit[7:0]: man_vts_adj_val[7:0]
0x382C	VTS ADJUST	0x20	RW	Bit[7:0]: r_threshold_vts_sub
0x382D	FSIN/VSYNC	0x04	RW	Bit[7:6]: Not used Bit[5]: r_fsync_pol Bit[4]: r_vsync_pol Bit[3:0]: fsin_glitch_filter_num
0x382E	EXPO OFFSET	0x01	RW	Bit[7:0]: r_exp_offset
0x382F	RSVD	–	–	Reserved
0x3830	R COUNT	–	R	Bit[7:0]: R counter[15:8]
0x3831	R COUNT	–	R	Bit[7:0]: R counter[7:0]

table 6-8 timing control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x3832	FSYNC	0x00	RW	Bit[7:0]: fsync_st[15:8]
0x3833	FSYNC	0x00	RW	Bit[7:0]: fsync_st[7:0]
0x3834	FSYNC	0x00	RW	Bit[7:0]: fsync_end[15:8]
0x3835	FSYNC	0x04	RW	Bit[7:0]: fsync_end[7:0]

6.9 OTP control [0x3D80 - 0x3D98, 0x3DA4]

table 6-9 OTP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3D80	OTP_PROGRAM_ CTRL	–	RW	Bit[7]: otp_pgenb_o 0: Not used 1: Program ongoing (read only) Bit[6:1]: Not used Bit[0]: OTP_program_enable Write 0 to 1 to start programming (write only)
0x3D81	OTP_LOA_CTRL	–	RW	Bit[7]: OTP_load_enable (read only) Bit[6]: Not used Bit[5]: OTP_bist_error (read only) Bit[4]: OTP_bist_done (read only) Bit[3]: Not used Bit[2]: bist_clr (write only) Bit[1]: autoload_m (write only) Bit[0]: OTP_rd 0: Not used 1: OTP load ongoing (read/write)
0x3D82	OTP_PGM_PULSE	0x32	RW	Bit[7:0]: Control program strobe pulse Unit: 8 × Tsclk
0x3D83	OTP_LOAD_PULSE	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: Control load strobe pulse Unit: 2 × Tsclk

table 6-9 OTP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3D84	OTP_MODE_CTRL	0x00	RW	Bit[7]: Program disable 0: Not used 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode Bit[5:1]: Not used Bit[0]: bank_sram_switch
0x3D85	OTP_REG85	0x1B	RW	Bit[7]: Not used Bit[6]: r_otp_bist_comp_val Bit[5]: otp_bist_select 0: Compare with SRAM 1: Compare with zero Bit[4]: OTP_bist_enable Bit[3]: OTP power up load data enable Bit[2]: OTP wake up load setting enable Bit[1]: OTP hardware load setting enable Bit[0]: OTP software load setting enable
0x3D86	SRAM_TEST_ SIGNALS	0x02	RW	Bit[7:3]: Not used Bit[2]: r_test Bit[1:0]: r_rm
0x3D87	OTP_PS2CS	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: ps_to_csb_time_control Unit: SCLK
0x3D88	OTP_START_ ADDRESS	0x00	RW	Bit[7:0]: start_high_addr for manual mode
0x3D89	OTP_START_ ADDRESS	0x00	RW	Bit[7:0]: start_low_addr for manual mode
0x3D8A	OTP_EN_ADDRESS	0x03	RW	Bit[7:0]: end_high_addr for manual mode
0x3D8B	OTP_END_ADDRESS	0xFF	RW	Bit[7:0]: end_low_addr for manual mode
0x3D8C	OTP_SETTING_STT_ ADDRESS	0x00	RW	Bit[7:0]: start_high_addr for load setting
0x3D8D	OTP_SETTING_STT_ ADDRESS	0x00	RW	Bit[7:0]: start_low_addr for load setting
0x3D8E	OTP CHECK ERROR	–	R	Bit[7:0]: otp_check_err_addr[15:8]
0x3D8F	OTP CHECK ERROR	–	R	Bit[7:0]: otp_check_err_addr[7:0]
0x3D90	R_BASE_ADR_H	0x00	RW	Bit[7:0]: efuse_base_addr[15:8]
0x3D91	R_BASE_ADR_L	0x00	RW	Bit[7:0]: efuse_base_addr[7:0]
0x3D92	PGENB_TIMING	0x1F	RW	Bit[7:4]: t_pgenb_end Bit[3:0]: t_pgenb_start

table 6-9 OTP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3D93	VDDQ_TIMING	0x46	RW	Bit[7:4]: t_vddq_end Bit[3:0]: t_vddq_start
0x3D94	OTP_CTRL	0x14	RW	Bit[7:0]: Gap between strobe pulse when programmed
0x3D95	OTP_CTRL	0x05	RW	Bit[7:4]: Not used Bit[3:0]: Gap between strobe pulse when loaded
0x3D96	OTP_CTRL	0x0E	RW	Bit[7:0]: SRAM_RM
0x3D97	OTP_CTRL	0x39	RW	Bit[7]: Not used Bit[6:0]: Address enable to load/program enable setup and hold time Unit: 2 × Tsclk
0x3D98	OTP_CTRL	0x62	RW	Bit[7:4]: Address to address enable hold time during program Unit: 2 × Tsclk Bit[3:0]: Address to address enable hold time during load Unit: 2 × Tsclk
0x3DA4	OTP_CTRL	0x04	RW	Bit[7:4]: Not used Bit[3:2]: slope_select 00: 0x 01: 1x 10: 2x 11: 3x (5us) Bit[1:0]: ef_slope_sreg

6.10 BLC [0x4000 - 0x401A, 0x4028 - 0x407F]

table 6-10 BLC registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x4000	BLC_TOP_0	0xF8	RW	Bit[7]: off_trig_en Bit[6]: exp_chg_trig_en Bit[5]: gain_chg_trig_en Bit[4]: fmt_chg_trig_en Bit[3]: rst_trig_en Bit[2]: man_trig Bit[1]: off_frz_en Bit[0]: off_always_up
0x4001	BLC_TOP_1	0x2B	RW	Bit[7]: zero_ln_out_en Bit[6]: blk_ln_out_en Bit[5]: dither_en Bit[4]: off_man_en Bit[3]: mf_en Bit[2]: one_channel_blc_en Bit[1]: dc_blc_en Bit[0]: blc_en
0x4002~ 0x4003	RSVD	–	–	Reserved
0x4004	BLC_TOP_4	0x00	RW	Bit[7:4]: Not used Bit[3:0]: blk_lvl_target_l[11:8]
0x4005	BLC_TOP_5	0x40	RW	Bit[7:0]: blk_lvl_target_l[7:0]
0x4006	BLC_TOP_6	0x00	RW	Bit[7:4]: Not used Bit[3:0]: hwin_pad[11:8]
0x4007	BLC_TOP_7	0x10	RW	Bit[7:0]: hwin_pad[7:0]
0x4008	BLC_TOP_8	0x00	RW	Bit[7:6]: Not used Bit[5:0]: bl_start[5:0]
0x4009	BLC_TOP_9	0x05	RW	Bit[7:6]: Not used Bit[5:0]: bl_end[5:0]
0x400A	BLC_TOP_A	0x02	RW	Bit[7:6]: Not used Bit[5:0]: off_lim_th[13:8]
0x400B	BLC_TOP_B	0x00	RW	Bit[7:0]: off_lim_th[7:0]
0x400C	BLC_TOP_C	0x00	RW	Bit[7:4]: Not used Bit[3:0]: hwin_off[11:8]
0x400D	BLC_TOP_D	0x10	RW	Bit[7:0]: hwin_off[7:0]
0x400E	BLC_TOP_E	0x00	RW	Bit[7]: Not used Bit[6:0]: mf_th[6:0]

table 6-10 BLC registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x400F	BLC_TOP_F	0x11	RW	Bit[7]: Not used Bit[6]: apply_gate_clk_en Bit[5]: offset_clk_gate_en Bit[4]: mf_clk_gate_en Bit[3]: target_output_option Bit[2]: set_zb Bit[1:0]: off_limit_cut_option[1:0]
0x4010	BLC_TOP_10	0x00	RW	Bit[7]: img_gfirst_rvs Bit[6]: blk_rblue_rvs Bit[5]: img_rblue_rvs Bit[4:3]: Not used Bit[2]: mf_gate_data_en Bit[1]: apply_gate_data_en Bit[0]: offset_gate_data_en
0x4011	BLC_TOP_11	0xFF	RW	Bit[7:6]: Not used Bit[5]: man_avg_en Bit[4]: off_chg_avg_en Bit[3]: fmt_chg_avg_en Bit[2]: gain_chg_avg_en Bit[1]: rst_avg_en Bit[0]: exp_chg_avg_en
0x4012	BLC_TOP_12	0x08	RW	Bit[7:0]: rst_trig_fn[7:0]
0x4013	BLC_TOP_13	0x02	RW	Bit[7:0]: fmt_manu_trig_fn[7:0]
0x4014	BLC_TOP_14	0x02	RW	Bit[7:0]: gain_exp_off_trig_fn[7:0]
0x4015	RSVD	–	–	Reserved
0x4016	BLC_TOP_16	0x00	RW	Bit[7:4]: Not used Bit[3:0]: off_trig_th[11:8]
0x4017	BLC_TOP_17	0x04	RW	Bit[7:0]: off_trig_th[7:0]
0x4018	RSVD	–	–	Reserved
0x4019	BLC_TOP_19	0x04	RW	Bit[7:0]: blk_ln_num[7:0]
0x401A	BLC_TOP_1A	0x58	RW	Bit[7]: h_size_man_en Bit[6]: kcoef_mirror Bit[5:3]: Not used Bit[2]: ln_num_man Bit[1:0]: byp_mode[1:0]
0x4028	BLC_TOP_28	0x4F	RW	Bit[7]: Not used Bit[6]: lim_bits_en Bit[5]: thres_en Bit[4]: thres_man_en Bit[3:0]: Not used

table 6-10 BLC registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x4029~ 0x402B	RSVD	–	–	Reserved
0x402C	BLC_TOP_2C	0x03	RW	Bit[7:4]: Not used Bit[3:0]: thres_man[11:8]
0x402D	BLC_TOP_2D	0xFF	RW	Bit[7:0]: thres_man[7:0]
0x402E~ 0x4031	RSVD	–	–	Reserved
0x4032	BLC_TOP_32	0x8E	RW	Bit[7:6]: output_bits[1:0] Bit[5]: input_10bits Bit[4]: kcoef_man_en Bit[3:1]: Not used Bit[0]: vsync_sel
0x4033	RSVD	–	–	Reserved
0x4034	BLC_TOP_34	0x00	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_b_man[9:8]
0x4035	BLC_TOP_35	0x80	RW	Bit[7:0]: kcoef_b_man[7:0]
0x4036	BLC_TOP_36	0x00	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_gb_man[9:8]
0x4037	BLC_TOP_37	0x80	RW	Bit[7:0]: kcoef_gb_man[7:0]
0x4038	BLC_TOP_38	0x00	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_gr_man[9:8]
0x4039	BLC_TOP_39	0x80	RW	Bit[7:0]: kcoef_gr_man[7:0]
0x403A	BLC_TOP_3A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_r_man[9:8]
0x403B	BLC_TOP_3B	0x80	RW	Bit[7:0]: kcoef_r_man[7:0]
0x403C~ 0x403F	RSVD	–	–	Reserved
0x4040	BLC_TOP_40	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_man0000[13:8]
0x4041	BLC_TOP_41	0x00	RW	Bit[7:0]: off_man0000[7:0]
0x4042	BLC_TOP_42	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_man0001[13:8]
0x4043	BLC_TOP_43	0x00	RW	Bit[7:0]: off_man0001[7:0]
0x4044	BLC_TOP_44	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_man0010[13:8]
0x4045	BLC_TOP_45	0x00	RW	Bit[7:0]: off_man0010[7:0]

table 6-10 BLC registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x4046	BLC_TOP_46	0x00	RW	Bit[7:6]: Not used Bit[5:0]: off_man0011[13:8]
0x4047	BLC_TOP_47	0x00	RW	Bit[7:0]: off_man0011[7:0]
0x4048~ 0x4049	RSVD	–	–	Reserved
0x4050	BLC_TOP_50	0x00	RW	Bit[7:0]: zl_start[7:0]
0x4051	BLC_TOP_51	0x05	RW	Bit[7:0]: zl_end[7:0]
0x4052~ 0x405B	RSVD	–	–	Reserved
0x405C	BLC_TOP_5C	0x20	RW	Bit[7:6]: Not used Bit[5:0]: off_avg_weight[5:0]
0x405D	BLC_TOP_5D	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rnd_gain_th[9:8]
0x405E	BLC_TOP_5E	0x00	RW	Bit[7:0]: rnd_gain_th[7:0]
0x405F~ 0x4064	RSVD	–	–	Reserved
0x4065	BLC_TOP_65	0x00	RW	Bit[7:2]: Not used Bit[1:0]: zero_ln_num[9:8]
0x4066	BLC_TOP_66	0x02	RW	Bit[7:0]: zero_ln_num[7:0]
0x4067~ 0x406D	RSVD	–	–	Reserved
0x406E	BLC_TOP_6E	0x00	RW	Bit[7:3]: Not used Bit[2:0]: h_size_man[10:8]
0x406F	BLC_TOP_6F	0x00	RW	Bit[7:0]: h_size_man[7:0]
0x4070~ 0x4071	RSVD	–	–	Reserved
0x4072	BLC_TOP_72	–	R	Bit[7]: Not used Bit[6:0]: Blcoffset0000[14:8]
0x4073	BLC_TOP_73	–	R	Bit[7:0]: Blcoffset0000[7:0]
0x4074~ 0x4075	RSVD	–	–	Reserved
0x4076	BLC_TOP_76	–	R	Bit[7]: Not used Bit[6:0]: Blcoffset0001[14:8]
0x4077	BLC_TOP_77	–	R	Bit[7:0]: Blcoffset0001[7:0]

table 6-10 BLC registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x4078~ 0x4079	RSVD	–	–	Reserved
0x407A	BLC_TOP_7A	–	R	Bit[7]: Not used Bit[6:0]: Blcoffset0010[14:8]
0x407B	BLC_TOP_7B	–	R	Bit[7:0]: Blcoffset0010[7:0]
0x407C~ 0x407D	RSVD	–	–	Reserved
0x407E	BLC_TOP_7E	–	R	Bit[7]: Not used Bit[6:0]: Blcoffset0011[14:8]
0x407F	BLC_TOP_7F	–	R	Bit[7:0]: Blcoffset0011[7:0]

6.11 format [0x4300 - 0x4302]

table 6-11 format registers

address	register name	default value	R/W	description
0x4300	CLIP MAX HI	0xFF	RW	Bit[7:0]: clip_max[11:4]
0x4301	CLIP MIN HI	0x00	RW	Bit[7:0]: clip_min[11:4]
0x4302	CLIP LO	0x0F	RW	Bit[7:4]: clip_min[3:0] Bit[3:0]: clip_max[3:0]

6.12 column ADC sync and SYNC_FIFO [0x4500 - 0x4505]

table 6-12 column ADC sync and SYNC_FIFO registers

address	register name	default value	R/W	description
0x4500	CTRL	0x0A	RW	Bit[7:6]: rblue_option Bit[5:0]: r_sync_fifo_sram_tst
0x4501	R1	0x00	RW	Bit[7]: r_skip_man_ctl Bit[6]: read_mem_alw Bit[5:4]: r_hbin4_opt 00: Average of 4 pixels 01: Summary of 4 pixels 10: Select first bin2 pixel 11: Select last bin2 pixel Bit[3:2]: r_hbin2_opt 00: Average 01: Summary 10: Select first pixel 11: Select last pixel Bit[1]: r_dat_swap Bit[0]: r_srclk_inv
0x4502	R2	0x00	RW	Bit[7:0]: r_data_offset
0x4503	R3	0x00	RW	Bit[7:0]: r_sync_fifo_start_pcnt[15:8]
0x4504	R4	0x06	RW	Bit[7:0]: r_sync_fifio_start_pcnt[7:0]
0x4505	R5	0x84	RW	Bit[7]: r_sync_fifo_bisclk_sel Bit[6:5]: Not used Bit[4]: r_blk_output_en Bit[3]: r_skip_rblue_dis Bit[2]: r_fix_start_eol Bit[1]: r_mir_man_en Bit[0]: r_mir_man

6.13 MIPI [0x4800, 0x4802 - 0x480C, 0x4810 - 0x4814, 0x4818 - 0x484F]

table 6-13 MIPI registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x4800	MIPI CTRL00	0x00	RW	Bit[7:6]: Reserved Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Not used Bit[2]: pclk_inv_o 0: Use falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Use rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[1]: first_bit Change clk_lane first bit 0: Output 0x55 1: Output 0xAA Bit[0]: LPX_select for PCLK domain 0: Auto calculate t_lpx_p Unit: pclk2x cycle 1: Use lpx_p_min[7:0]

table 6-13 MIPI registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x4802	MIPI CTRL02	0x00	RW	Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare Unit: pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare Unit: pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post Unit: pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail Unit: pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit Unit: pclk2x 1: Use hs_exit_min_o[7:0] Bit[2] hs_zero_sel 0: Auto calculate T_hs_zero Unit: pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail Unit: pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero Unit: pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL03	0x00	RW	Bit[7:5]: Not used Bit[4]: fifo_rd_spd_o Bit[3]: manu_ofset_o t_perio manual offset SMIA Bit[2]: r_manu_half2one t_period half to 1 SMIA Bit[1:0]: Reserved
0x4804	NOT USED	–	–	Not Used

table 6-13 MIPI registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x4805	MIPI CTRL05	0x00	RW	Bit[7:4]: Not used Bit[3]: lpda_retim_manu_o Bit[2]: lpda_retim_sel_o 0: Not used 1: Manual Bit[1]: lpck_retim_manu_o Bit[0]: lpck_retim_sel_o 0: Not used 1: Manual
0x4806	MIPI CTRL06	0x00	RW	Bit[7:5]: Not used Bit[4]: pu_mark_en_o Power up mark1 enable Bit[3]: mipi_remot_rst Bit[2]: mipi_susp Bit[1]: smia_lane_ch_en Bit[0]: tx_lsb_first 0: High bit first 1: Low power transmit low bit first
0x4807	MIPI CTRL07	0x03	RW	Bit[7:4]: Not used Bit[3:0]: sw_t_lpx ul_tx T_lpx
0x4808	MIPI CTRL08	0x18	RW	Bit[7:0]: wkup_dly Mark1 wakeup delay/2^10
0x4809	MIPI CTRL09	0x04	RW	Bit[7]: hcnt_end_man_en 0: Not used 1: Use r_hcnt_end_man Bit[6]: cs_cnt_end_man 0: Not used 1: cs_cnt rolls over as it reaches r_hcnt_end_man Bit[5:0]: pkt_start_offset
0x480A	MIPI CTRL0A	0x00	RW	Bit[7:0]: r_hcnt_end_man[15:8]
0x480B	MIPI CTRL0B	0x00	RW	Bit[7:0]: r_hcnt_end_man[7:0]
0x480C	MIPI CTRL0B	0x12	RW	Bit[7]: mipi_pkt_start_man Use pkt_start_offset as packet start offset Bit[6:4]: r_mask_ln_num Real masked line number is 2 × r_mask_ln_num Bit[3:0]: fifo_start_size
0x4810	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[15:8] Maximum frame counter of frame sync short packet

table 6-13 MIPI registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x4811	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[7:0] Maximum frame counter of frame sync short packet
0x4812	NOT USED	–	–	Not Used
0x4813	MIPI CTRL13	0x00	RW	Bit[7:3]: Not used Bit[2]: vc_sel Bit[1:0] VC ID
0x4814	MIPI CTRL14	0x2A	RW	Bit[7]: Not used Bit[6]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data type Bit[5:0]: dt_man Manual data type
0x4818	HS ZERO MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_zero_min[9:8] Minimum value of hs_zero Unit: ns
0x4819	HS ZERO MIN	0x70	RW	Bit[7:0]: hs_zero_min[7:0] Minimum value of hs_zero Unit: ns hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_trail_min[9:8] Minimum value of hs_trail Unit: ns
0x481B	HS TRAIL MIN	0x3C	RW	Bit[7:0]: hs_trail_min[7:0] Minimum value of hs_trail Unit: ns hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK ZERO MIN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: clk_zero_min[9:8] Minimum value of clk_zero Unit: ns
0x481D	CLK ZERO MIN	0x2C	RW	Bit[7:0]: clk_zero_min[7:0] Minimum value of clk_zero Unit: ns clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o

table 6-13 MIPI registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x481E	CLK PREPARE MAX	0x5F	RW	Bit[7:0]: clk_prepare_max[7:0] Maximum value of clk_prepare Unit: ns
0x481F	CLK PREPARE MIN	0x26	RW	Bit[7:0]: clk_prepare_min[7:0] Minimum value of clk_prepare Unit: ns clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK POST MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_post_min[9:8] Minimum value of clk_post Unit: ns
0x4821	CLK POST MIN	0x3C	RW	Bit[7:0]: clk_post_min[7:0] Minimum value of clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	CLK TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_trail_min[9:8] Minimum value of clk_trail Unit: ns
0x4823	CLK TRAIL MIN	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Minimum value of clk_trail Unit: ns clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX P MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: lpx_p_min[9:8] Minimum value of lpx_p Unit: ns
0x4825	LPX P MIN	0x32	RW	Bit[7:0]: lpx_p_min[7:0] Minimum value of lpx_p Unit: ns lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	HS PREPARE MIN	0x32	RW	Bit[7:0]: hs_prepare_min[7:0] Minimum value of hs_prepare Unit: ns
0x4827	HS PREPARE MAX	0x55	RW	Bit[7:0]: hs_prepare_max[7:0] Maximum value of hs_prepare Unit: ns hs_prepare_real = hs_prepare_max_o + Tui*ui_hs_prepare_max_o

table 6-13 MIPI registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x4828	HS EXIT MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_exit_min[9:8] Minimum value of hs_exit Unit: ns
0x4829	HS EXIT MIN	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Minimum value of hs_exit Unit: ns hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	UI HS ZERO MIN	0x06	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_zero_min[5:0] Minimum UI value of hs_zero Unit: UI
0x482B	UI HS TRAIL MIN	0x04	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_trail_min[5:0] Minimum UI value of hs_trail Unit: UI
0x482C	UI CLK ZERO MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_zero_min[5:0] Minimum UI value of clk_zero Unit: UI
0x482D	UI CLK PREPARE	0x00	RW	Bit[7:4]: ui_clk_prepare_max Maximum UI value of clk_prepare Unit: UI Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare Unit: UI
0x482E	UI CLK POST MIN	0x34	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_post_min[5:0] Minimum UI value of clk_post Unit: UI
0x482F	UI CLK TRAIL MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_trail_min[5:0] Minimum UI value of clk_trail Unit: UI
0x4830	UI LPX P MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_lpx_p_min[5:0] Minimum UI value of lpx_p (pclk2x domain) Unit: UI

table 6-13 MIPI registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x4831	UI HS PREPARE	0x64	RW	Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepares Unit: UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare Unit: UI
0x4832	UI HS EXIT MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_exit_min[5:0] Minimum UI value of hs_exit Unit: UI
0x4833	MIPI PKT STAR SIZE	0x10	RW	Bit[7:6]: Not used Bit[5:0]: mipi_pkt_star_size[5:0]
0x4834~ 0x4836	NOT USED	–	–	Not Used
0x4837	PCLK PERIOD	0x0E	RW	Bit[7:0]: pclk_period[7:0] Period of pclk2x, pclk_div = 1 and 1-bit decimal
0x4838	MIPI LP GPIO0	0x00	RW	Bit[7]: lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6]: lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4]: lp_n0_o Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2]: lp_dir_man1 0: Input 1: Output Bit[1]: lp_p1_o Bit[0]: lp_n1_o

table 6-13 MIPI registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x4839	MIPI LP GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o
0x483A~ 0x483B	NOT USED	–	–	Not Used
0x483C	MIPI CTRL3C	0x02	RW	Bit[7:4]: Not used Bit[3:0]: t_clk_pre Unit pclk2x cycle
0x483D	MIPI LP GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use lp_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1_o Bit[0]: lp_ck_n1_o
0x483E~ 0x4847	NOT USED	–	–	Not Used
0x4848	SEL_MIPI_CTRL48	–	R	Bit[7:0]: mipi_fcnt[15:8]

table 6-13 MIPI registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x4849	SEL_MIPI_CTRL_49	–	R	Bit[7:0]: mipi_fcnt[7:0]
0x484A	SEL MIPI CTRL4A	0x3F	RW	Bit[7:6]: Not used Bit[5]: slp_lp_pon_man_o set for power up Bit[4]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck Bit[2]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	SMIA OPTION	0x07	RW	Bit[7:2]: Not used Bit[1]: clk_start_sel_o 0: Clock starts after start of frame 1: Clock starts after reset Bit[0]: sof_sel_o 0: Frame starts after HREF occurs 1: Frame starts after start of frame
0x484C	SEL MIPI CTRL4C	0x00	RW	Bit[7:4]: Not used Bit[3]: smia_fcnt_i select Bit[2]: prbs_enable Bit[1]: hs_test_only MIPI high speed only test mode enable Bit[0]: set_frame_cnt_0 Set frame count to inactive mode (set to 0)
0x484D	TEST PATTERN DATA	0xB6	RW	Bit[7:0]: test_patten_data[7:0] Data lane test pattern
0x484E	FE DLY	0x10	RW	Bit[7:0]: fe_dly Last packet to frame end delay/2
0x484F	TEST PATTERN CK DATA	0x55	RW	Bit[7:2]: Not used Bit[1:0]: clk_test_patten_reg

6.14 ISPFC [0x4900 - 0x4903]

table 6-14 ISPFC registers

address	register name	default value	R/W	description
0x4900	R0	0x00	RW	Bit[7:4]: Not used Bit[3]: sof_after_line0 Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4901	R1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_on_number
0x4902	R2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_off_number
0x4903	R3	0x00	RW	Bit[7]: zero_line_mask_dis Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.15 DSP [0x5000 - 0x502C, 0x502E - 0x5038, 0x5041 - 0x5049]

table 6-15 DSP registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP_CTRL_0	0xED	RW	Bit[7]: WIN enable Bit[6]: Not used Bit[5]: DPC enable Bit[4]: OTP enable Bit[3:2]: Not used Bit[1]: PD bypass enable Bit[0]: ISP enable
0x5001	ISP_CTRL_1	0x07	RW	Bit[7:4]: Not used Bit[3]: Control signal latch mode Bit[2]: Not used Bit[1]: PD pixel check enable Bit[0]: rst_protect enable
0x5002	RSVD	–	–	Reserved

table 6-15 DSP registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5003	ISP_CTRL_3	0x00	RW	Bit[7]: SOF select Bit[6]: EOF select Bit[5:4]: Manual CFA pattern Bit[3:1]: Not used Bit[0]: CFA pattern manual mode
0x5004	ISP_CTRL_4	0x00	RW	Bit[7:3]: Not used Bit[2]: PD location manual mode Bit[1]: Image size manual mode Bit[0]: ISP module work manual mode
0x5005	ISP_CTRL_5	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nMF option
0x5006~ 0x5011	RSVD	–	–	Reserved
0x5012	ISP_CTRL_18	0x10	RW	Bit[7:5]: Reserved Bit[4:0]: Manual Hsize[12:8]
0x5013	ISP_CTRL_19	0x80	RW	Bit[7:0]: Manual Hsize[7:0]
0x5014	ISP_CTRL_20	0x0C	RW	Bit[7:4]: Reserved Bit[3:0]: Manual Vsize[11:8]
0x5015	ISP_CTRL_21	0x40	RW	Bit[7:0]: Manual Hsize[7:0]
0x5016	ISP_CTRL_22	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Manual L m_nPDCycleX
0x5017	ISP_CTRL_23	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Manual L m_nPDCycleY
0x5018	ISP_CTRL_24	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nPDY
0x5019	ISP_CTRL_25	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nPDX1
0x501A	ISP_CTRL_26	0x0A	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nPDX2
0x501B	ISP_CTRL_27	0x06	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nPDX3
0x501C	ISP_CTRL_28	0x0E	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nPDX4
0x501D	RSVD	–	–	Reserved
0x501E	ISP_CTRL_30	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual L m_nWinXStart[11:8]
0x501F	ISP_CTRL_31	0x40	RW	Bit[7:0]: Manual L m_nWinXStart[7:0]

table 6-15 DSP registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5020	ISP_CTRL_32	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual L m_nWinYStart[11:8]
0x5021	ISP_CTRL_33	0x40	RW	Bit[7:0]: Manual L m_nWinYStart[7:0]
0x5022	ISP_CTRL_34	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: Manual L m_nWinWidth[12:8]
0x5023	ISP_CTRL_35	0x80	RW	Bit[7:0]: Manual L m_nWinWidth[7:0]
0x5024	ISP_CTRL_36	0x0B	RW	Bit[7:4]: Reserved Bit[3:0]: Manual L m_nWinHeight[11:8]
0x5025	ISP_CTRL_37	0x40	RW	Bit[7:0]: Manual L m_nWinHeight[7:0]
0x5026	ISP_CTRL_38	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Manual S m_nPDCycleX
0x5027	ISP_CTRL_39	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Manual S m_nPDCycleY
0x5028	ISP_CTRL_40	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nPDY
0x5029	ISP_CTRL_41	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nPDX1
0x502A	ISP_CTRL_42	0x0A	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nPDX2
0x502B	ISP_CTRL_43	0x06	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nPDX3
0x502C	ISP_CTRL_44	0x0E	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nPDX4
0x502D	RSVD	–	–	Reserved
0x502E	ISP_CTRL_46	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual S m_nWinXStart[11:8]
0x502F	ISP_CTRL_47	0x40	RW	Bit[7:0]: Manual S m_nWinXStart[7:0]
0x5030	ISP_CTRL_48	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual S m_nWinYStart[11:8]
0x5031	ISP_CTRL_49	0x40	RW	Bit[7:0]: Manual S m_nWinYStart[7:0]
0x5032	ISP_CTRL_50	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: Manual S m_nWinWidth[12:8]
0x5033	ISP_CTRL_51	0x80	RW	Bit[7:0]: Manual S m_nWinWidth[7:0]
0x5034	ISP_CTRL_52	0x0B	RW	Bit[7:4]: Reserved Bit[3:0]: Manual S m_nWinHeight[11:8]

table 6-15 DSP registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5035	ISP_CTRL_53	0x40	RW	Bit[7:0]: Manual S m_nWinHeight[7:0]
0x5036	ISP_CTRL_54	0x00	RW	Bit[7]: dis_ck_gt_win Bit[6]: Not used Bit[5]: dis_ck_gt_dpc Bit[4]: dis_ck_gt_pd_byp Bit[3]: dis_ck_gt_otp Bit[2:1]: Not used Bit[0]: dis_ck_gt_top
0x5037	ISP_CTRL_55	0x00	RW	Bit[7:3]: Not used Bit[2]: dis_ck_gt_vblank Bit[1]: dis_ck_gt_hblank Bit[0]: dis_ck_gt_all
0x5038	ISP_CTRL_56	0x00	RW	Bit[7:6]: Not used Bit[5:2]: Read margin input Bit[1]: Read margin enable Bit[0]: SRAM test1
0x5041	ISP_CTRL_65	0x08	RW	Bit[7:0]: Sensor control register from ISP to sensor
0x5042	ISP_CTRL_66	0x08	RW	Bit[7:0]: Sensor control register from ISP to sensor
0x5043	ISP_CTRL_67	0x84	RW	Bit[7:0]: Sensor control register from ISP to sensor
0x5044	ISP_CTRL_68	0x62	RW	Bit[7:0]: Sensor control register from ISP to sensor
0x5045	ISP_CTRL_69	0x20	RW	Bit[7:0]: Sensor control register from ISP to sensor
0x5046	ISP_CTRL_70	0x20	RW	Bit[7:0]: Sensor control register from ISP to sensor
0x5047	ISP_CTRL_71	0xA4	RW	Bit[7:0]: Sensor control register from ISP to sensor
0x5048	ISP_CTRL_72	0x20	RW	Bit[7:0]: Sensor control register from ISP to sensor
0x5049	ISP_CTRL_73	0xA4	RW	Bit[7:0]: Sensor control register from ISP to sensor

6.16 pre_ISP [0x5080 - 0x508C, 0x50A0 - 0x50AF, 0x50B2 - 0x50B5]

table 6-16 pre_ISP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5080	ISP_CTRL_0	0x00	RW	Bit[7]: Test pattern enable 0: Disable 1: Enable Bit[6]: Rolling enable (rolling bar in test mode) 0: Disable 1: Enable Bit[5]: Transparent effect enable 0: Disable 1: Enable Bit[4]: Black/white or color square selection 0: Color 1: black/white Bit[3:2]: Color bar style Bit[1:0]: Test mode select
0x5081	ISP_CTRL_1	0x01	RW	Bit[7:2]: Not used Bit[1]: win_cut_en Bit[0]: isp_test
0x5082	ISP_CTRL_2	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Line number interrupt[12:8]
0x5083	ISP_CTRL_3	0x01	RW	Bit[7:0]: Line number interrupt[7:0]
0x5084~ 0x508B	RSVD	–	–	Reserved
0x508C	ISP_CTRL_12	0x03	RW	Bit[7:2]: Not used Bit[1]: Mirror option Bit[0]: Flip option
0x50A0	ISP_CTRL_32	–	R	Bit[7:4]: X odd inc[3:0] Bit[3:0]: Y odd inc[3:0]
0x50A1	ISP_CTRL_33	–	R	Bit[7:5]: Not used Bit[4:0]: X offset[12:8]
0x50A2	ISP_CTRL_34	–	R	Bit[7:0]: X offset[7:0]
0x50A3	ISP_CTRL_35	–	R	Bit[7:4]: Not used Bit[3:0]: Y offset[11:8]
0x50A4	ISP_CTRL_36	–	R	Bit[7:0]: Y offset[7:0]
0x50A5	ISP_CTRL_37	–	R	Bit[7:5]: Not used Bit[4:0]: Win X offset[12:8]
0x50A6	ISP_CTRL_38	–	R	Bit[7:0]: Win X offset[7:0]

table 6-16 pre_ISP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x50A7	ISP_CTRL_39	–	R	Bit[7:4]: Not used Bit[3:0]: Win Y offset[11:8]
0x50A8	ISP_CTRL_40	–	R	Bit[7:0]: Win Y offset[7:0]
0x50A9	ISP_CTRL_41	–	R	Bit[7:5]: Not used Bit[4:0]: Win X output size[12:8]
0x50AA	ISP_CTRL_42	–	R	Bit[7:0]: Win X output size[7:0]
0x50AB	ISP_CTRL_43	–	R	Bit[7:4]: Not used Bit[3:0]: Win Y output size[11:8]
0x50AC	ISP_CTRL_44	–	R	Bit[7:0]: Win Y output size[7:0]
0x50AD	ISP_CTRL_45	–	R	Bit[7:6]: Reserved Bit[5:4]: X skip Bit[3:2]: Reserved Bit[1:0]: Y skip
0x50AE	ISP_CTRL_46	–	R	Bit[7:4]: X even inc[3:0] Bit[3:0]: Y even inc[3:0]
0x50AF	ISP_CTRL_47	–	R	Bit[7:4]: Reserved Bit[3]: X odd inc[4] Bit[2]: Y odd inc[4] Bit[1]: X even inc[4] Bit[0]: Y even inc[4]
0x50B2	ISP_CTRL_50	–	R	Bit[7:5]: Not used Bit[4:0]: Pixel number[12:8]
0x50B3	ISP_CTRL_51	–	R	Bit[7:0]: Pixel number[7:0]
0x50B4	ISP_CTRL_52	–	R	Bit[7:4]: Not used Bit[3:0]: Line number[11:8]
0x50B5	ISP_CTRL_53	–	R	Bit[7:0]: Line number[7:0]

6.17 DPC [0x5180 - 0x51A6, 0x5200 - 0x521F]

table 6-17 DPC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5180~ 0x51A6	OTP CTRL	–	–	OTP Control Registers
0x5200	ISP_CTRL_0	0x1B	RW	Bit[7]: Enable tail Bit[6]: Enable tailing cluster Bit[5]: Enable 3x3 cluster Bit[4]: Enable saturate cross cluster Bit[3]: Enable cross cluster Bit[2]: Manual mode enable Bit[1]: Black pixel enable Bit[0]: White pixel enable
0x5201	ISP_CTRL_1	0x94	RW	Bit[7:6]: Vertical number list[2] Bit[5:4]: Vertical number list[1] Bit[3:2]: Vertical number list[0] Bit[1]: Enable G clip Bit[0]: Enable share buffer
0x5202	ISP_CTRL_2	0x2E	RW	Bit[7:6]: Not used Bit[5:4]: Bayer pattern order Bit[3:2]: Image boundary extend options Bit[1:0]: Vertical number list[3]
0x5203	ISP_CTRL_3	0x24	RW	Bit[7]: Not used Bit[6:3]: White pixel threshold list[0] Bit[2:0]: Maximum vertical number
0x5204	ISP_CTRL_4	0x12	RW	Bit[7:4]: White pixel threshold list[2] Bit[3:0]: White pixel threshold list[1]
0x5205	ISP_CTRL_5	0x41	RW	Bit[7:4]: Dark pixel threshold ratio Bit[3:0]: White pixel threshold list[3]
0x5206	ISP_CTRL_6	0x48	RW	Bit[7:4]: Status threshold Bit[3:0]: Cluster threshold
0x5207	ISP_CTRL_7	0x84	RW	Bit[7:4]: Pattern match threshold Bit[3:0]: Status threshold step
0x5208	ISP_CTRL_8	0x40	RW	Bit[7:4]: Adaptive pattern step Bit[3:0]: Adaptive pattern threshold
0x5209	ISP_CTRL_9	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Saturate pixel threshold for clusters
0x520A	ISP_CTRL_10	0x03	RW	Bit[7:5]: Not used Bit[4:0]: Gain threshold list[0]
0x520B	ISP_CTRL_11	0x0F	RW	Bit[7:5]: Not used Bit[4:0]: Gain threshold list[1]

table 6-17 DPC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x520C	ISP_CTRL_12	0x1F	RW	Bit[7:5]: Not used Bit[4:0]: Gain threshold list[2]
0x520D	ISP_CTRL_13	0x0F	RW	Bit[7:0]: DPC level list[0]
0x520E	ISP_CTRL_14	0xFD	RW	Bit[7:0]: DPC level list[1]
0x520F	ISP_CTRL_15	0xF5	RW	Bit[7:0]: DPC level list[2]
0x5210	ISP_CTRL_16	0xF5	RW	Bit[7:0]: DPC level list[3]
0x5211~ 0x5213	RSVD	–	–	Reserved
0x5214	ISP_CTRL_20	0x00	RW	Bit[7]: Recover clock gate disable Bit[6]: Recover clock gate disable Bit[5]: Recover clock gate disable Bit[4]: SRAM clock gate disable Bit[3]: Buffer control clock gate disable Bit[2]: Start frame clock gate disable Bit[1]: Clock gate disable Bit[0]: Pixel order manual enable
0x5215~ 0x5217	RSVD	–	–	Reserved
0x5218	ISP_CTRL_24	–	R	Bit[7]: Not used Bit[6:0]: Bthre
0x5219	ISP_CTRL_25	–	R	Bit[7:5]: Not used Bit[4:0]: Wthre
0x521A	ISP_CTRL_26	–	R	Bit[7:5]: Not used Bit[4:0]: Thre1
0x521B	ISP_CTRL_27	–	R	Bit[7:0]: Thre2
0x521C	ISP_CTRL_28	–	R	Bit[7]: Not used Bit[6:0]: Thre3
0x521D	ISP_CTRL_29	–	R	Bit[7]: Not used Bit[6:0]: Thre4
0x521E	ISP_CTRL_30	–	R	Bit[7:4]: Level Bit[3:0]: Pconnected
0x521F	ISP_CTRL_31	–	R	Bit[7:3]: Not used Bit[2:0]: Vnum

7 operating specifications

7.1 absolute maximum ratings

table 7-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	1.8V
	V_{DD-IO}	4.5V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 functional temperature

table 7-2 functional temperature

parameter	range
operating temperature (for applications up to 30 fps)[a]	-30°C to +85°C junction temperature
stable image temperature[b]	0°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

7.3 DC characteristics

table 7-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max[a]	unit
supply					
V_{DD-A}	supply voltage (analog)	2.7	2.8	2.9	V
V_{DD-D}	supply voltage (digital core for 2-lane MIPI up to 900 Mbps/lane)	1.14	1.2	1.26	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	1.9	V
I_{DD-A}	active (operating) current[b]		35.7		mA
I_{DD-IO}			0.4		mA
I_{DD-D}[c]			78		mA
$I_{DDS-SCCB}$	standby current[d]		1		mA
$I_{DDS-XSHUTDN}$			2		µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[e]	SCL and SDA	-0.5	0	0.54	V
V_{IH}	SCL and SDA	1.28	1.8	3.0	V

a. maximum active current is measured under typical supply voltage

b. DVDD is provided by the external regulator. DVDD and EVDD are tied together. DOVDD = 1.8V

c. data is based on ISP ON

d. standby current is measured at room temperature with external clock off

e. based on DOVDD = 1.8V

7.4 timing characteristics

figure 7-1 reference clock input timing diagram

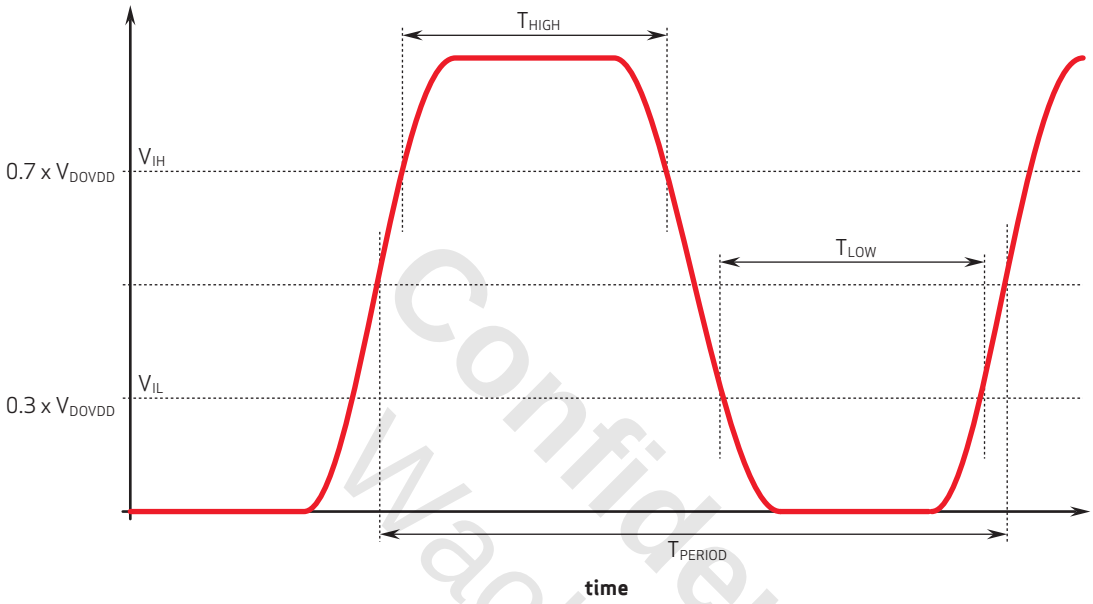


table 7-4 timing characteristics

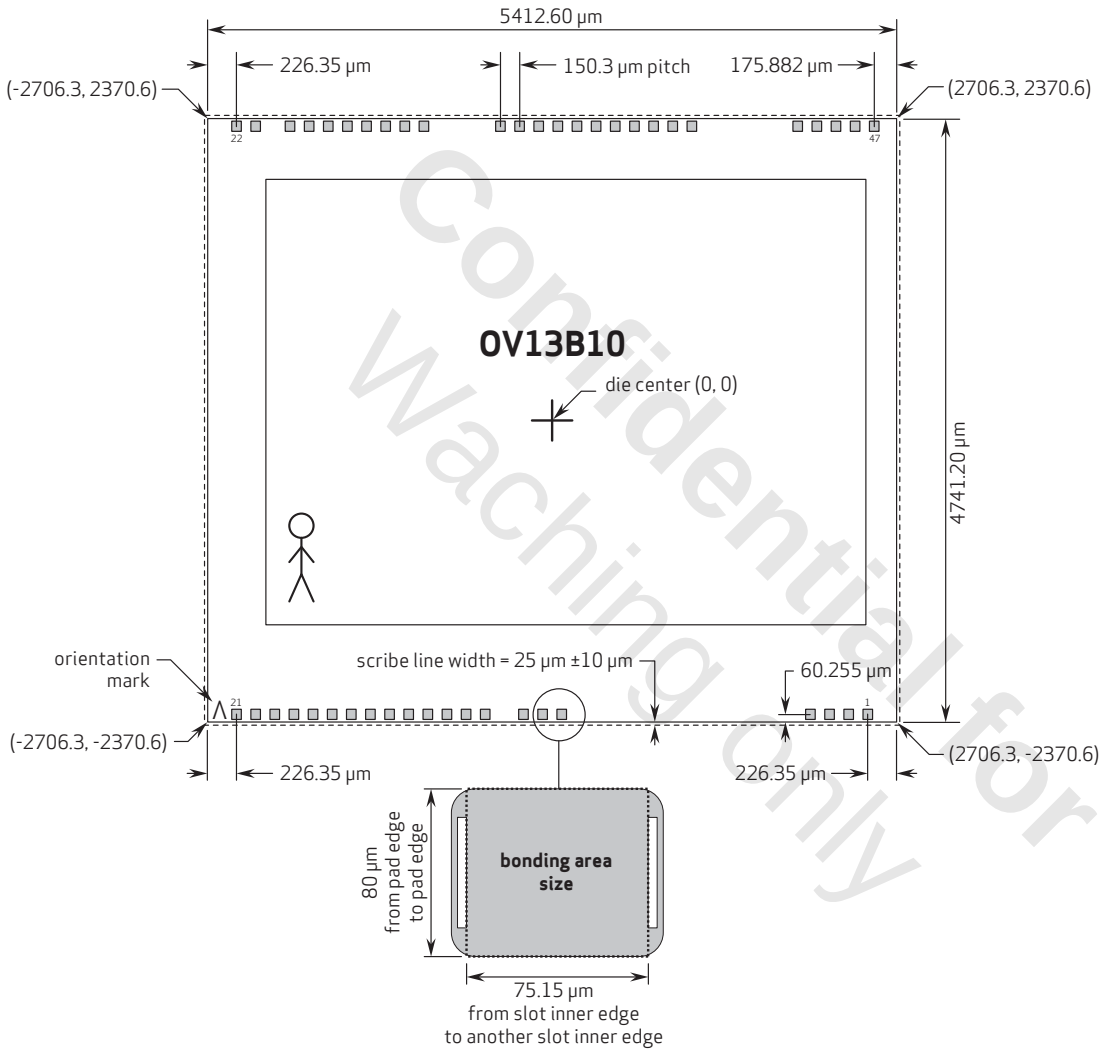
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{EXTCLK}	frequency (EXTCLK)[a]	6	24	64	MHz
T_{PERIOD}	period (EXTCLK)	15.6	41.7	166.7	ns
T_{LOW}	low level width (EXTCLK)	0.35×T_{PERIOD}		0.65×T_{PERIOD}	ns
T_{HIGH}	high level width (EXTCLK)	0.35×T_{PERIOD}		0.65×T_{PERIOD}	ns

a. for input clock range 6~64MHz, the OV13B10 can tolerate input clock period jitter up to 600ps peak-to-peak

8 mechanical specifications

8.1 COB physical specifications

figure 8-1 COB die specifications



note 1 all dimensions and coordinates are in µm unless otherwise specified

note 2 bonding outside the defined bonding area is prohibited as it may cause failure in reliability or functionality

table 8-1 pad location coordinates (sheet 1 of 2)

pad number	pad name	x coordinate	y coordinate	bonding area size
1	AGND	2479.950	-2310.345	75.15x80
2	AVDD	2329.650	-2310.345	75.15x80
3	DOGND	2179.350	-2310.345	75.15x80
4	DVDD	2029.050	-2310.345	75.15x80
5	DVDD	75.150	-2310.345	75.15x80
6	DOGND	-75.150	-2310.345	75.15x80
7	ATEST	-225.450	-2310.345	75.15x80
8	VSYNC	-526.050	-2310.345	75.15x80
9	SCL	-676.350	-2310.345	75.15x80
10	SDA	-826.650	-2310.345	75.15x80
11	EXTCLK	-976.950	-2310.345	75.15x80
12	FSIN	-1127.250	-2310.345	75.15x80
13	TM	-1277.550	-2310.345	75.15x80
14	XSHUTDN	-1427.850	-2310.345	75.15x80
15	DOVDD	-1578.150	-2310.345	75.15x80
16	DOGND	-1728.450	-2310.345	75.15x80
17	DVDD	-1878.750	-2310.345	75.15x80
18	AVDD	-2029.050	-2310.345	75.15x80
19	AGND	-2179.350	-2310.345	75.15x80
20	DOGND	-2329.650	-2310.345	75.15x80
21	DVDD	-2479.950	-2310.345	75.15x80
22	DVDD	-2479.950	2310.345	75.15x80
23	DOGND	-2329.650	2310.345	75.15x80
24	MDN3	-2059.650	2310.345	75.15x80
25	MDP3	-1909.350	2310.345	75.15x80
26	MDN1	-1759.050	2310.345	75.15x80
27	MDP1	-1608.750	2310.345	75.15x80
28	EVDD	-1458.450	2310.345	75.15x80
29	EGND	-1308.150	2310.345	75.15x80
30	MCN	-1157.850	2310.345	75.15x80
31	MCP	-1007.550	2310.345	75.15x80

table 8-1 pad location coordinates (sheet 2 of 2)

pad number	pad name	x coordinate	y coordinate	bonding area size
32	PVDD	-406.350	2310.345	75.15x80
33	EGND	-256.050	2310.345	75.15x80
34	EVDD	-105.750	2310.345	75.15x80
35	MDN0	44.550	2310.345	75.15x80
36	MDP0	194.850	2310.345	75.15x80
37	MDN2	345.150	2310.345	75.15x80
38	MDP2	495.450	2310.345	75.15x80
39	DOGND	646.722	2310.345	75.15x80
40	DVDD	797.022	2310.345	75.15x80
41	DOVDD	947.322	2310.345	75.15x80
42	SID	1097.622	2310.345	75.15x80
43	VH	1929.218	2310.345	75.15x80
44	VN2	2079.518	2310.345	75.15x80
45	VN	2229.818	2310.345	75.15x80
46	AVDD	2380.118	2310.345	75.15x80
47	AGND	2530.418	2310.345	75.15x80

8.2 reconstructed wafer (RW) physical specifications

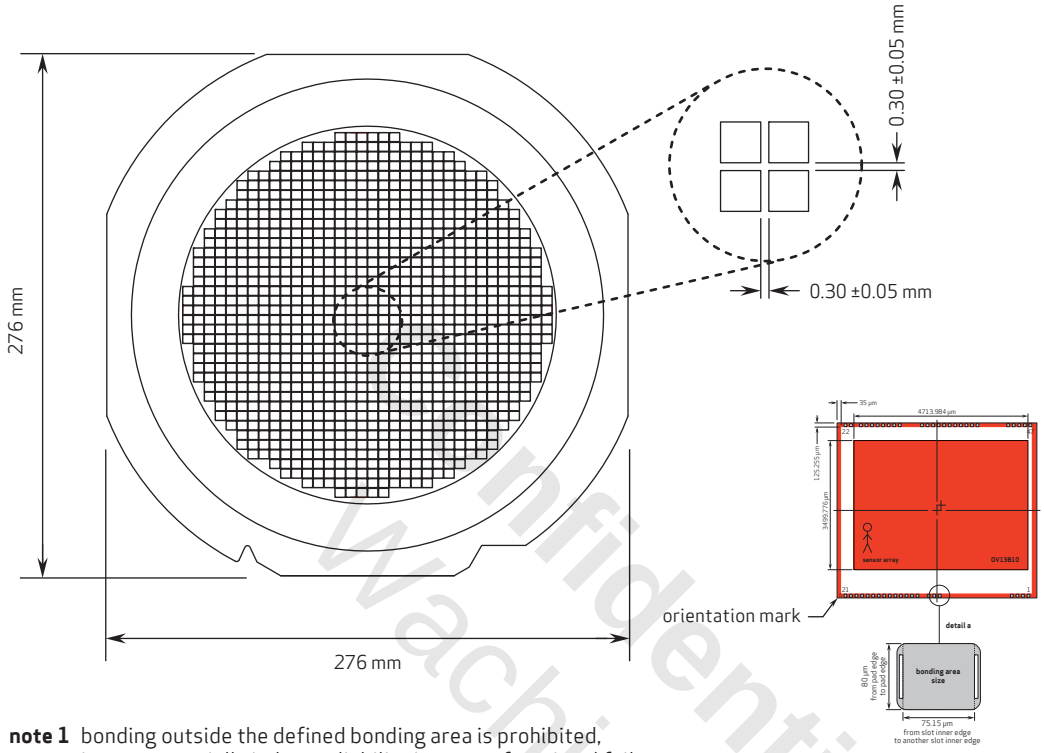
- maximum total die count: 987
- film frame: Compact Disco Stainless SUS420
- carrier tape: UV tape

note
Actual die count varies and the absent die may be less than 10% of the maximum total die count (excluding the last frame of the wafer lot).

table 8-2 RW physical dimensions

feature	dimensions
RW physical dimensions	8" RW on 12" frame
wafer thickness (OVXXXXX-ABCD)	
C=5	150 µm ± 10 µm (5.9 mil ± 0.4 mil)
reconstructed wafer street width	300 µm ± 50 µm (11.8 mil ± 2 mil)
placement accuracy x, y, theta	± 50 µm (± 2 mil), <1.0 degree
singulated die size	
width	5462.6 µm ± 20 µm (215.06 mil ± 0.8 mil)
length	4791.2 µm ± 20 µm (188.63 mil ± 0.8 mil)
bond pad size	89.1 µm × 80.1 µm (3.51 mil × 3.15 mil)
minimum bond pad pitch	150.3 µm (5.9 mil)
bonding area size	75.15 µm × 80 µm (2.96 mil × 3.1 mil)
optical array	
die center	(0, 0)
optical center from die center	107.901 µm, 143.073 µm (4.2 mil, 5.6 mil)

figure 8-2 OV13B10 RW physical diagram



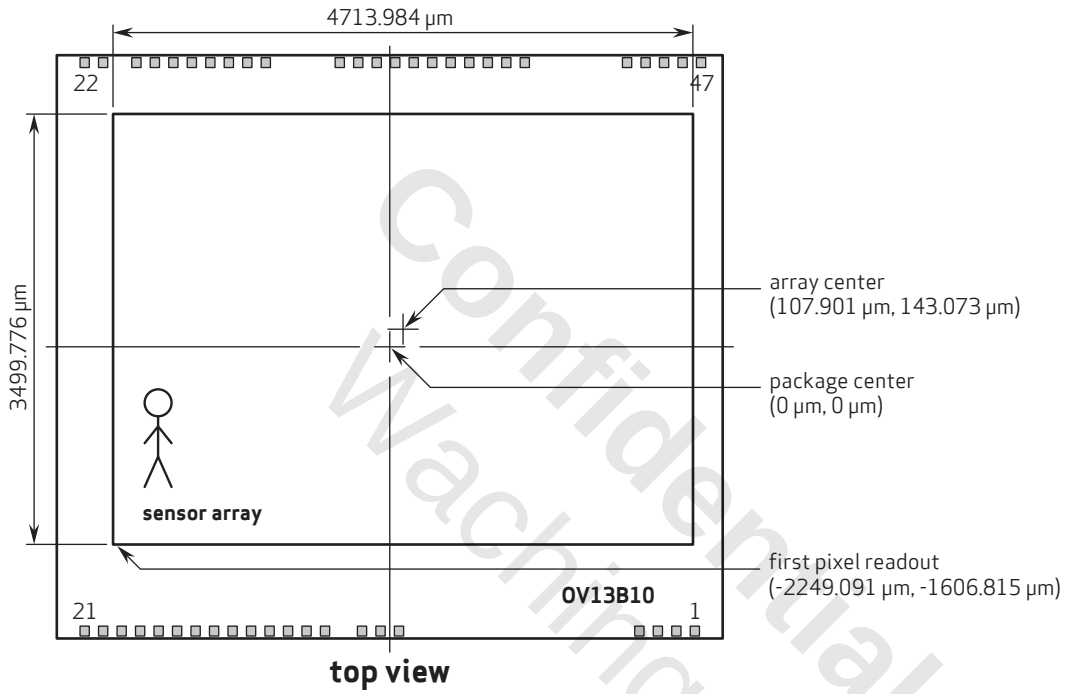
note 1 bonding outside the defined bonding area is prohibited, it may potentially induce reliability issues or functional failure

note 2 keep-out-of-contact areas are highlighted in red color for related process fixtures/tools (e.g., nozzles, collets, etc.)

9 optical specifications

9.1 sensor array center

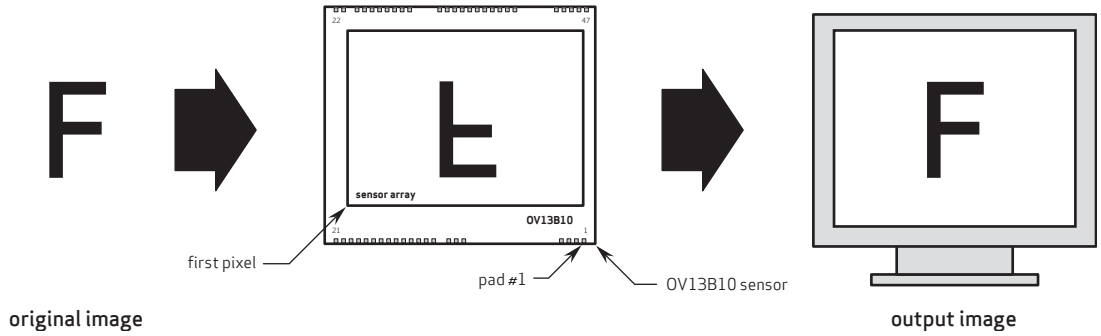
figure 9-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies flip image, chip is typically mounted as above with first pixel at bottom-left corner.

figure 9-2 final image output



9.2 lens chief ray angle (CRA)

figure 9-3 chief ray angle (CRA)

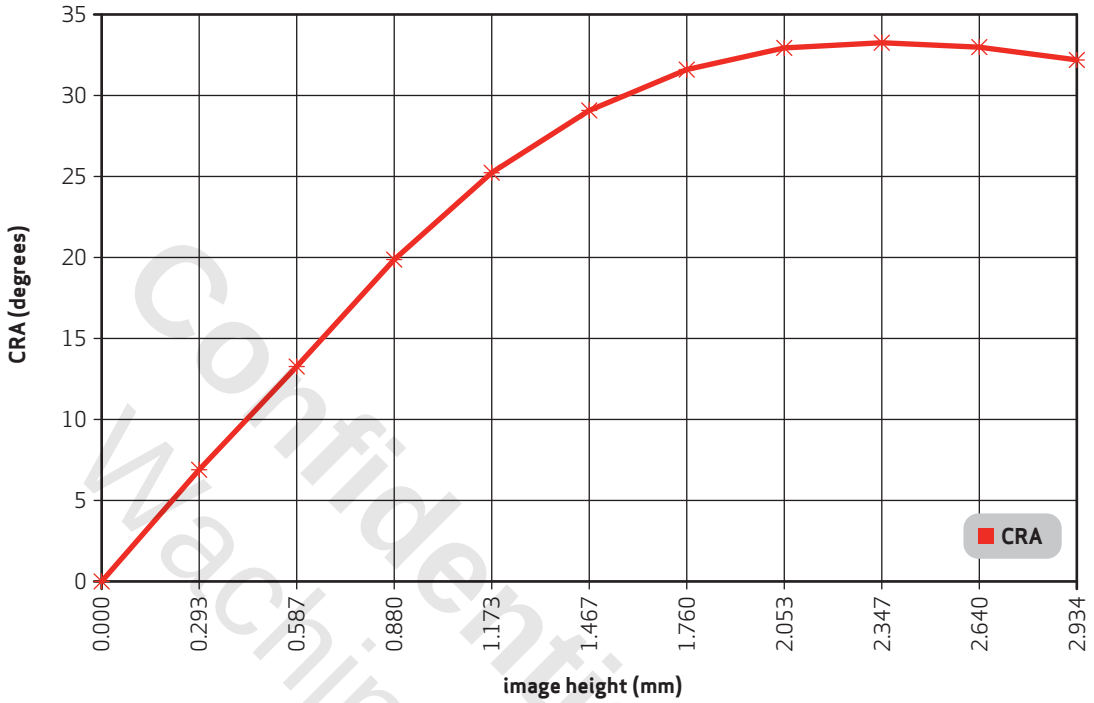


table 9-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0.0	0.000	0.00
0.1	0.293	7.00
0.2	0.587	13.30
0.3	0.880	19.90
0.4	1.173	25.23
0.5	1.467	29.08
0.6	1.760	31.60
0.7	2.053	32.91
0.8	2.347	33.25
0.9	2.640	33.00
1.0	2.934	32.20

appendix A handling of RW devices

A.1 ESD /EOS prevention

1. Ensure that there is 500V ESD control in all work areas.
2. Use ESD safety shoes, ground strap, and static control smocks in test areas.
3. Use grounded work carts and tables in inspection areas.
4. OmniVision recommends the use of ionized air in all work areas.

A.2 particles and cleanliness of environment

1. All production, inspection and packaging areas should meet Class10 environment requirements.
2. Use optical microscopes with 50X and 100X magnifications for particle inspection.
3. Ensure that there is good cassette sealing for particle protection during storage.
4. OmniVision recommends water cleaning to remove removable particles.
5. RW die should be stored in nitrogen gas purged cabinets with temperature less than 30°C and relative humidity of 60% before assembly.

A.3 other requirements

1. Reliability assurance of RW or COB bare die is certified by product reliability of the bare die in a CLCC, CSP or QFP package form factor. Precautions should be taken if the packaging form factor of the bare die is other than these specified.
2. Avoid exposure to strong sunlight for extended periods of time as the color filter of the image sensor may become discolored.
3. Avoid direct exposure of the sensor bare die to high temperature and/or humidity environment as sensor characteristics will be affected. Extra precautions should be exercised if the bare die experiences temperatures exceeding 260°C for more than 75 seconds.

revision history

version 1.0 11.14.2018

- initial release

version 1.1 12.21.2018

- in key specifications, changed maximum image transfer rate for 1080p to 60 fps and changed minimum exposure to 4 lines
- in table 2-1, changed 10-bit MIPI data rate (default) for 13.2 Mpixel and 10 Mpixel to 4-lane @ 1120 Mbps/lane, changed 10-bit MIPI data rate (default) for 3.3 Mpixel, 1080p, and 720p to 4-lane @ 560 Mbps/lane, and changed frame rate for 1080p to 60 fps
- in section 2.9.1, changed first sentence of first paragraph to "PLL1 generates a default 140 MHz pixel clock and 560 MHz MIPI serial clock from a 6~64 MHz input clock."
- in section 2.9.2, changed first sentence of first paragraph to "PLL2 generates a default 112 MHz system clock from a 6~64 MHz input clock." and updated figure 2-6
- in section 3.1, changed second sentence of fourth paragraph to "Maximum exposure time is VTS-8 and minimum exposure time is 4 lines."
- in section 3.5, added third sentence to end of first paragraph
- in table 3-1, changed description of register bit 0x3820[5] to "Black line vertical flip control; 0: Normal; 1: Vertical flip", changed description of register bit 0x3820[4] to "Image vertical flip enable; 0: Normal; 1: Vertical flip", and changed description of register bit 0x3820[3] to "Image horizontal mirror disable; 0: Image horizontal mirror enable; 1: Normal"
- in table 4-1, changed description of register bit 0x3820[5] to "Black line vertical flip control; 0: Digital gain (ISP use)...; 1: Vertical flip", changed description of register bit 0x3820[4] to "Image vertical flip enable; 0: Normal; 1: Vertical flip", and changed description of register bit 0x3820[3] to "Image horizontal mirror disable; 0: Image horizontal mirror enable; 1: Normal"
- in section 4.4, changed second sentence of first paragraph to "All 512 bytes are reserved for OmniVision.", removed first and second sentence of fourth paragraph, and changed first sentence of fifth paragraph to "The OTP memory access conditions are based on typical conditions: sensor wakeup, 2.8V AVDD, 1.2V DVDD, and 112 MHz system clock."
- in table 4-4, added row for 0x7010 and removed all rows for 0x7xxx
- in section 5.4, changed second sentence of first paragraph to "The exposure values in registers 0x3500 ~ 0x3502 are in units of one line and must be applied by group function.", changed fourth sentence of first paragraph to "The OV13B10 has a maximum 15.5x analog gain which is controlled by register 0x3508 ~ 0x3509,...", added fifth sentence to end of first paragraph, and changed sidebar note to "Maximum exposure = (VTS-8) lines, minimum exposure = 4 lines."
- in table 5-3, changed description of register bit 0x3503[6] to "dig_gain_delay option; 0: Digital gain (ISP use)..."; 1: Digital gain (ISP use)...", changed description of register bit 0x3503[4] to "gain_delay option; 0: Sensor/real gain..."; 1: Sensor/real gain...", removed description of register bits 0x3503[2:0], removed description of register bits 0x350A[3:2], and changed description of register bits 0x350A[1:0] to "dig_gain_coarse_b"
- in table 5-4, changed description of register bit 0x3503[6] to "dig_gain_delay option; 0: Digital gain (ISP use)..."; 1: Digital gain (ISP use)...", changed description of register bit 0x3503[4] to "gain_delay option; 0: Sensor/real gain..."; 1: Sensor/real gain...", removed description of register

bits 0x3503[2:0], removed description of register bits 0x350A[3:2], and changed description of register bits 0x350A[1:0] to "dig_gain_coarse_b"

- in table 6-2, changed default value for 0x300A to 0x56, changed default value for 0x300B to 0x0D, and changed default value for 0x300C to 0x42
- in table 6-5, changed description of register bit 0x3503[6] to "dig_gain_delay option; 0: Digital gain (ISP use)..."; 1: Digital gain (ISP use)...", changed description of register bit 0x3503[4] to "gain_delay option; 0: Sensor/real gain..."; 1: Sensor/real gain...", changed description of register bits 0x3503[2:0] to "Reserved", changed description of register bits 0x350A[7:2] to "Not used", and changed description of register bits 0x350A[1:0] to "dig_gain_coarse_b"
- in table 6-8, changed description of register bit 0x3820[5] to "Black line vertical flip control; 0: Normal; 1: Vertical flip", changed description of register bit 0x3820[4] to "Image vertical flip enable; 0: Normal; 1: Vertical flip", and changed description of register bit 0x3820[3] to "Image horizontal mirror disable; 0: Image horizontal mirror enable; 1: Normal"

version 1.11 01.28.2019

- in key specifications, changed active power requirements to 194mW, changed standby power requirements to 1mW and changed XSHUTDN power requirements to 1µW
- in table 4-2, changed description of register 0x380E to Bit[6:0]: VTS[14:8], Total vertical timing size
- in table 6-8, changed description of register 0x380E to Bit[7]: Reserved, Bit[6:0]: VTS[14:8], Total vertical timing size
- in table 7-3, changed typ value for I_{DD-A} to 34mA, changed typ value for I_{DD-IO} to 0.4mA, changed typ value for I_{DD-D} to 82mA, changed typ value for $I_{DDS-SCCB}$ to 1mA, and changed typ value for $I_{DDS-XSHUTDN}$ to 2µA

version 1.12 02.11.2019

- in table 9-1, changed 0.5 field (%) CRA (degrees) to 29.08 and 0.6 field (%) CRA (degrees) to 31.60

version 1.13 02.26.2019

- in table 7-3, changed typ value for supply symbol I_{DD-A} to 35.7 mA and changed typ value for supply symbol I_{DD-D} to 78 mA

version 1.14 03.20.2019

- in key specifications, replaced TBDs for sensitivity, max S/N ratio, and dynamic range
- in section 3.5, updated figure 3-4

Future in Sight®

OmniVision Technologies, Inc.

UNITED STATES

4275 Burton Drive
Santa Clara, CA 95054
tel: +1 408 567 3000
Chicago +1 847 508 0217
Detroit +1 248 919 6900
Optics Division +1 303 449 5593

UNITED KINGDOM

Hants +44 1252 761601

GERMANY

Munich +49 89 6381 9988

CHINA

Shanghai + 86 21 6175 9888
+86 21 6154 8000
Beijing + 86 10 8642 4200
Shenzhen + 86 755 8435 9733
Wuhan +86 27 5975 7800
Xian +86 29 8885 2537

INDIA

Bangalore +91 80 4112 8966

KOREA

Seoul + 82 2 3472 3769

JAPAN

Yokohama +81 45 478 7977
Kyoto +81 75 708 5352

NORWAY

Oslo +47 2295 8100

SINGAPORE +65 6933 1933

TAIWAN

Taipei +886 2 2657 9800
Hsin-chu +886 3 5656688

website: **www.ovt.com**