SONY

Diagonal 5.867 mm (Type 1/3.06) 13Mega-Pixel CMOS Image Sensor with Square Pixel for Camera

IMX258-0AMH5-C

General description and application

IMX258-0AMH5-C is a diagonal 5.867mm (Type 1/3.06) 13 Mega-pixel CMOS active pixel type stacked image sensor with a square pixel array. It adopts Exmor RS™ technology to achieve high speed image capturing by column parallel A/D converter circuits and high sensitivity and low noise image (comparing with conventional CMOS image sensor) through the backside illuminated imaging pixel structure. By introducing spatially varying exposure technology, high dynamic range still pictures and movies are achievable. It equips an electronic shutter with variable integration time. It operates with three power supply voltages: analog 2.7 V, digital 1.2 V and 1.8 V for input/output interface and achieves low power consumption.
In addition, this product is designed for use in cellular phone and tablet pc. When using this for another application, Sony does not guarantee the quality and reliability of product. Therefore, don't use this for applications other than cellular phone and tablet pc. Consult your Sony sales representative if you have any questions.

Functions and Features

- Back-illuminated and stacked CMOS image sensor Exmor RS™
- High Dynamic Range (HDR) mode with raw data output.
- High signal to noise ratio (SNR).
- Full resolution @30fps (Normal / HDR). 4K2K @30fps (Normal / HDR) 1080p @60fps (Normal)
- Output video format of RAW10/8.
- Pixel binning readout and V sub-sampling function.
- Independent flipping and mirroring.
- CSI-2 serial data output (MIPI 2lane/4lane, Max. 1.3Gbps/lane, D-PHY spec. ver. 1.1 compliant)
- 2-wire serial communication.
- Dynamic Defect Pixel Correction.
- Fast mode transition. (on the fly)
- Dual sensor synchronization operation.
- 4K bit of OTP ROM for users.
- Built-in temperature sensor

Exmor RS

Device Structure

◆CMOS image sensor
◆Image size : Diagonal 5.867 mm (Type 1/3.06)
◆Total number of pixels : 4224 (H) × 3192 (V) approx. 13.48 M pixels
◆Number of effective pixels : 4224 (H) × 3144 (V) approx. 13.28 M pixels
◆Number of active pixels : 4208 (H) × 3120 (V) approx. 13.13 M pixels
◆Chip size : 5.990 mm (H) × 3.908 mm (V)
◆Unit cell size : 1.12 µm (H) × 1.12 µm (V)
◆Substrate material : Silicon

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	-0.3 to +3.3	V	refer to VSS level
Supply voltage (digital)	VDIG	-0.3 to +1.8	V	
Supply voltage (interface)	VIF	-0.3 to +3.3	V	
Input voltage (digital)	VI	-0.3 to +3.3	V	
Output voltage (digital)	VO	-0.3 to +3.3	V	
Guaranteed Operating temperature	TOPR	-20 to +70	˚C	
Guaranteed storage temperature	TSTG	-30 to +80	˚C	
Guaranteed performance temperature	TSPEC	-20 to +60	˚C	

Recommended Operating Voltage

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	2.7 +0.2/-0.1	V	refer to VSS level
Supply voltage (digital)	VDIG	1.2 ± 0.1	V	
Supply voltage (interface)	VIF	1.8 ± 0.1	V	

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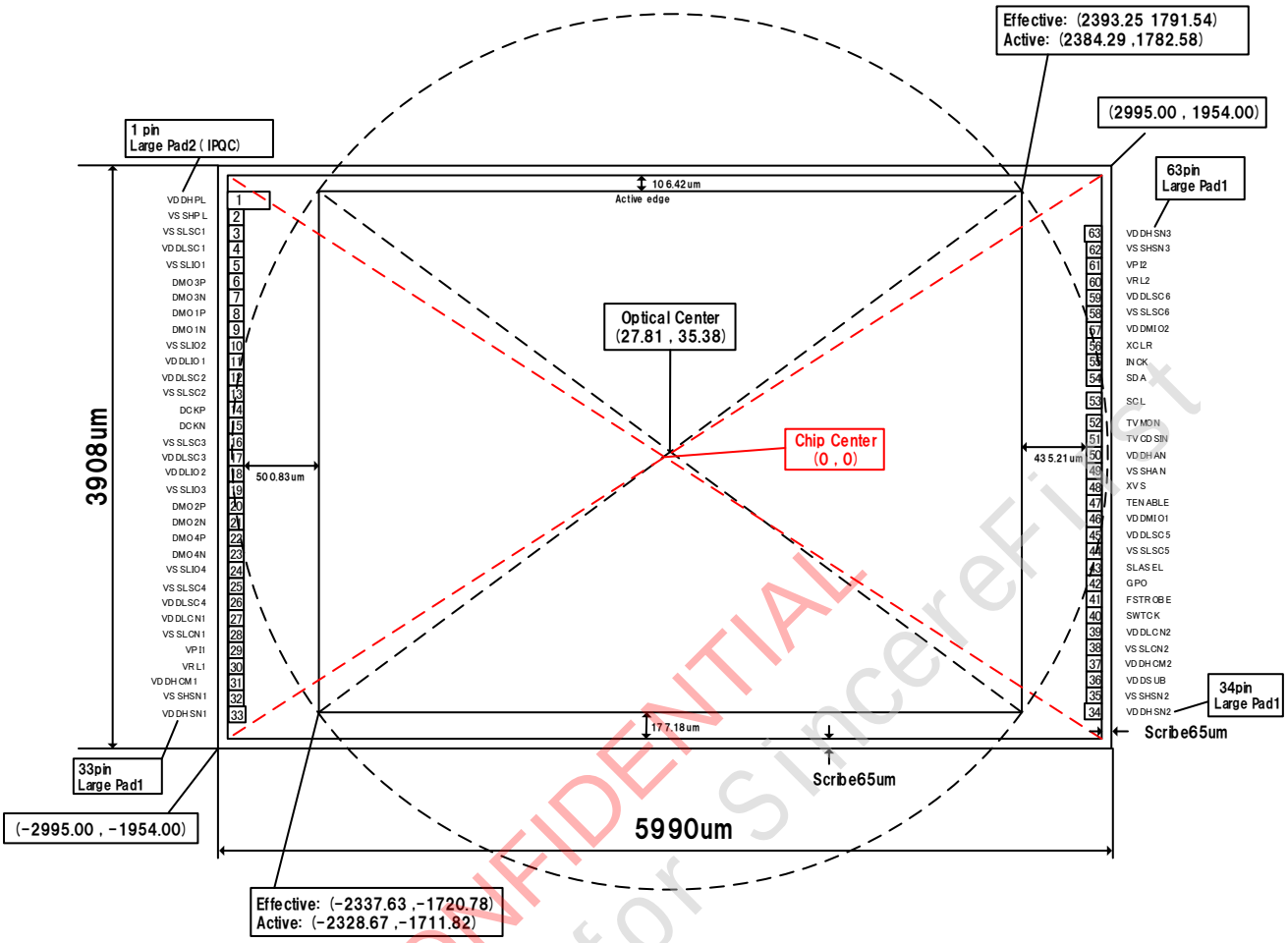
General-0.0.8

Contents

1. Chip Center and Optical Center



*1 Actual size of a chip will be smaller than indicated when dicing (scribe) is taken into account.

*2 Some PADs are located in image circle.

Figure 1 Chip Center and Optical Center (x and y coordinates in µm)

2. Pin Coordinates

Table 1 Pin Coordinates

No.	Symbol	X	Y
1	VDDHPL	-2855.00	1719.37
2	VSSHPL	-2873.25	1607.87
3	VSSLSC1	-2873.25	1500.35
4	VDDLSC1	-2873.25	1392.83
5	VSSLIO1	-2873.25	1285.31
6	DMO3P	-2873.25	1177.79
7	DMO3N	-2873.25	1070.27
8	DMO1P	-2873.25	962.75
9	DMO1N	-2873.25	855.23
10	VSSLIO2	-2873.25	747.71
11	VDDLIO1	-2873.25	640.19
12	VDDLSC2	-2873.25	532.67
13	VSSLSC2	-2873.25	425.15
14	DCKP	-2873.25	317.63
15	DCKN	-2873.25	210.11
16	VSSLSC3	-2873.25	102.59
17	VDDLSC3	-2873.25	-4.93
18	VDDLIO2	-2873.25	-112.45
19	VSSLIO3	-2873.25	-219.97
20	DMO2P	-2873.25	-327.49
21	DMO2N	-2873.25	-435.01
22	DMO4P	-2873.25	-542.53
23	DMO4N	-2873.25	-650.05
24	VSSLIO4	-2873.25	-757.57
25	VSSLSC4	-2873.25	-865.09
26	VDDLSC4	-2873.25	-972.61
27	VDDLCN1	-2873.25	-1080.13
28	VSSLCN1	-2873.25	-1187.65
29	VPI1	-2873.25	-1295.17
30	VRL1	-2873.25	-1402.69
31	VDDHCM1	-2873.25	-1510.21
32	VSSHSN1	-2873.25	-1617.73
33	VDDHSN1	-2867.25	-1725.25

No.	Symbol	X	Y
34	VDDHSN2	2867.25	-1695.25
35	VSSHSN2	2873.25	-1587.73
36	VDDSUB	2873.25	-1480.21
37	VDDHCM2	2873.25	-1372.69
38	VSSLCN2	2873.25	-1265.17
39	VDDLCN2	2873.25	-1157.65
40	SWTCK	2873.25	-1050.13
41	FSTROBE	2873.25	-942.61
42	GPO	2873.25	-835.09
43	SLASEL	2873.25	-727.57
44	VSSLSC5	2873.25	-620.05
45	VDDLSC5	2873.25	-512.53
46	VDDMIO1	2873.25	-405.01
47	TENABLE	2873.25	-297.49
48	XVS	2873.25	-189.97
49	VSSHAN	2873.25	-82.45
50	VDDHAN	2873.25	25.07
51	TVCDSIN	2873.25	132.59
52	TVMON	2873.25	240.11
53	SCL	2873.25	377.87
54	SDA	2873.25	515.63
55	INCK	2873.25	645.09
56	XCLR	2873.25	752.61
57	VDDMIO2	2873.25	860.13
58	VSSLSC6	2873.25	967.65
59	VDDLSC6	2873.25	1075.17
60	VRL2	2873.25	1182.69
61	VPI2	2873.25	1290.21
62	VSSHSN3	2873.25	1397.73
63	VDDHSN3	2867.25	1505.25

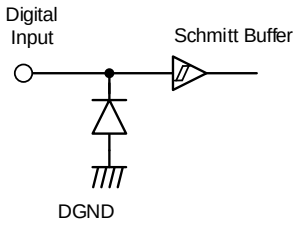
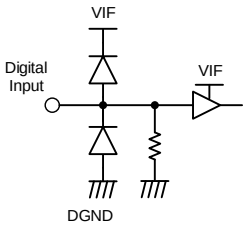
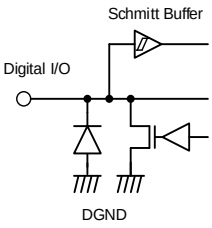
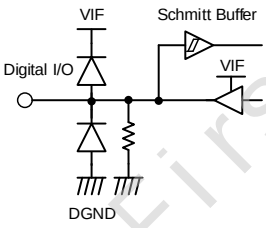
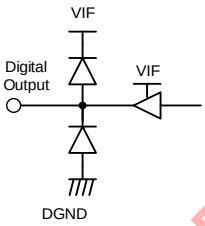
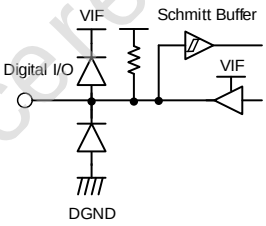
3. Pin Description

Table 2 Pin Description

No.	Symbol	I/O	A/D	Description	Remarks
1	VDDHPL	Power	A	VANA power supply	
2	VSSHPL	GND	A	VANA GND	
3	VSSLSC1	GND	D	VDIG GND	
4	VDDLSC1	Power	D	VDIG power supply	
5	VSSLIO1	GND	D	VDIG GND	
6	DMO3P	O	D	Digital output	MIPI output (DATA+)
7	DMO3N	O	D	Digital output	MIPI output (DATA–)
8	DMO1P	O	D	Digital output	MIPI output (DATA+)
9	DMO1N	O	D	Digital output	MIPI output (DATA–)
10	VSSLIO2	GND	D	VDIG GND	
11	VDDLIO1	Power	D	VDIG power supply	
12	VDDLSC2	Power	D	VDIG power supply	
13	VSSLSC2	GND	D	VDIG GND	
14	DCKP	O	D	Digital output	MIPI output (CLK+)
15	DCKN	O	D	Digital output	MIPI output (CLK–)
16	VSSLSC3	GND	D	VDIG GND	
17	VDDLSC3	Power	D	VDIG power supply	
18	VDDLIO2	Power	D	VDIG power supply	
19	VSSLIO3	GND	D	VDIG GND	
20	DMO2P	O	D	Digital output	MIPI output (DATA+)
21	DMO2N	O	D	Digital output	MIPI output (DATA–)
22	DMO4P	O	D	Digital output	MIPI output (DATA+)
23	DMO4N	O	D	Digital output	MIPI output (DATA–)
24	VSSLIO4	GND	D	VDIG GND	
25	VSSLSC4	GND	D	VDIG GND	
26	VDDLSC4	Power	D	VDIG power supply	
27	VDDLCN1	Power	D	VDIG power supply	
28	VSSLCN1	GND	D	VDIG GND	
29	VPI1	Power	A	VANA power supply	Connect VPI2
30	VRL1	Minus	A	Analog input	Connect VRL2
31	VDDHCM1	Power	A	VANA power supply	
32	VSSHSN1	GND	A	VANA GND	
33	VDDHSN1	Power	A	VANA power supply	
34	VDDHSN2	Power	A	VANA power supply	
35	VSSHSN2	GND	A	VANA GND	
36	VDDSUB	Power	A	VANA power supply	
37	VDDHCM2	Power	A	VANA power supply	
38	VSSLCN2	GND	D	VDIG GND	
39	VDDLCN2	Power	D	VDIG power supply	
40	SWTCK	I	D	Digital input	NC (pull-down)
41	FSTROBE	O	D	Digital output	Flash strobe
42	GPO	I/O	D	Digital I/O	Pull-down
43	SLASEL	I	D	Digital input	I2C slave address select Pull-down
44	VSSLSC5	GND	D	VDIG GND	
45	VDDLSC5	Power	D	VDIG power supply	
46	VDDMIO1	Power	D	VIF power supply	
47	TENABLE	I	D	Digital input	NC (pull-down)
48	XVS	I/O	D	Digital I/O	Pull-up

No.	Symbol	I/O	A/D	Description	Remarks
49	VSSHAN	GND	A	VANA GND	
50	VDDHAN	Power	A	VANA power supply	
51	TVCDSIN	I	A	Analog input	NC
52	TVMON	O	A	Analog output	NC
53	SCL	I/O	D	Digital I/O	I^2C pin
54	SDA	I/O	D	Digital I/O	I^2C pin
55	INCK	I	D	Digital input	Clock input
56	XCLR	I	D	Digital input	Chip clear (pull-down)
57	VDDMIO2	Power	D	VIF power supply	
58	VSSLSC6	GND	D	VDIG GND	
59	VDDLSC6	Power	D	VDIG power supply	
60	VRL2	Minus	A	Analog input	Connect VRL1
61	VPI2	Power	A	VANA power supply	Connect VPI1
62	VSSHSN3	GND	A	VANA GND	
63	VDDHSN3	Power	A	VANA power supply	

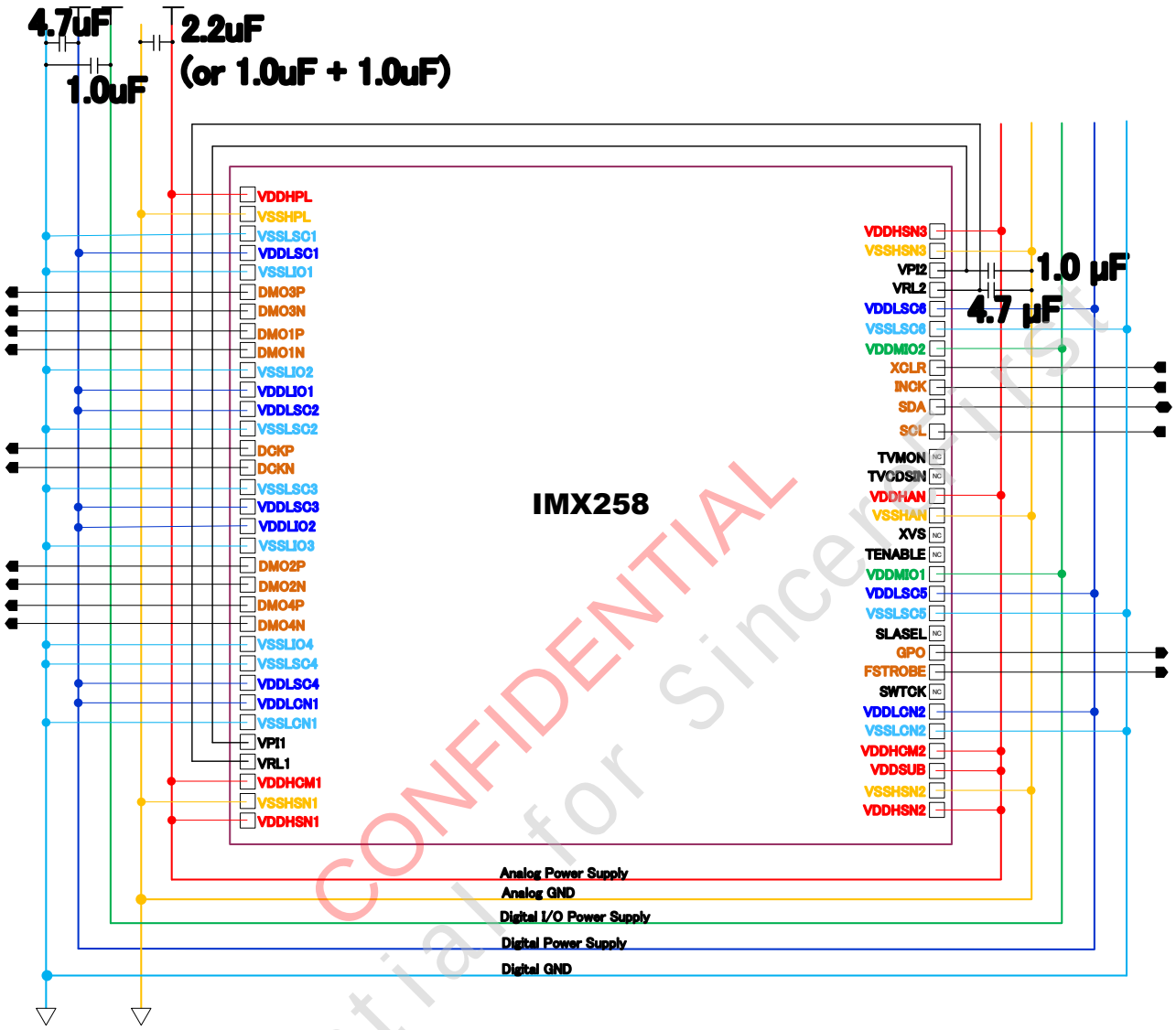
4. Input / Output Equivalent Circuit

Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
INCK		XCLR SLASEL	
SCL SDA		GPO	
FSTROBE		XVS	

VIF : 1.8 V power supply
DGND : VDIG GND

Figure 2 Input / Output Equivalent Circuit

5. Peripheral Circuit Diagram



Note : When fixing the potential of the chip back side, connect it to digital GND.

Note: The capacitor values and parts count used for decoupling of power supply lines in this diagram are determined only with Sony's testing environment. The capacitor values and/or parts count for power line decoupling may have to be reviewed and optimized by each manufacture depending on their design.

Figure 3 Peripheral Circuit (Recommended schematics)

6. Functional Description

6-1 System Outline

IMX258-0AMH5-C is a CMOS active pixel type image sensor which adopts the Exmor RS™ technology to achieve high sensitivity, low noise, and high speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, digital amplifier, image binning circuit, timing control circuit for imaging size and frame rate, CSI2 image data high speed serial interface,
PLL oscillator, and serial communication interface to control these functions.
Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.
A onetime programmable memory is embedded in the chip for storing the user data. It has 4 K-bit for users, 8 K-bit as a whole.

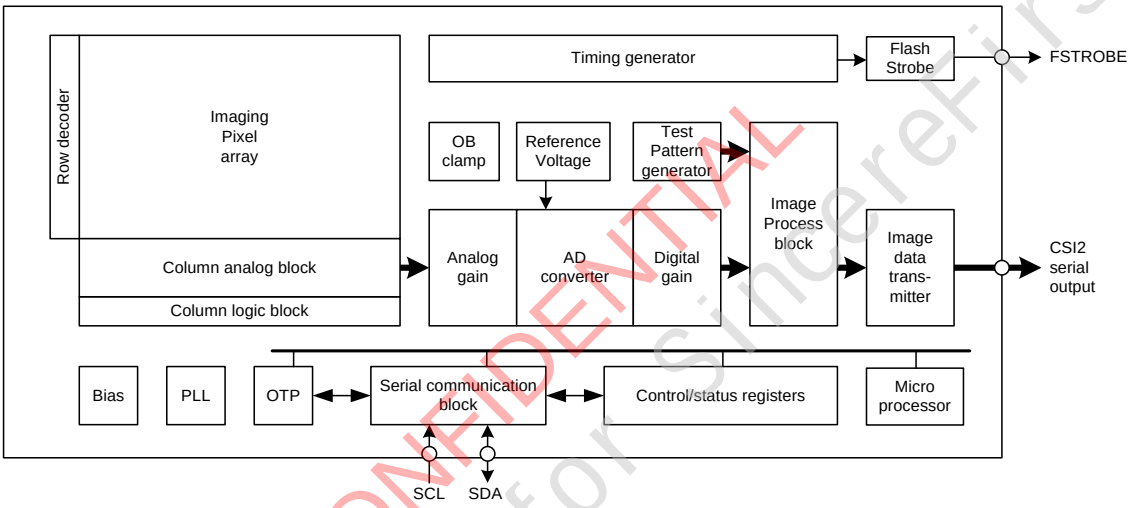


Figure 4 Overview of functional block diagram

6-2 Control register setting by the serial communication

The IMX258-0AMH5-C can use the 2-wire serial communication method for sensor control. These specifications are described for sensor control using the 2-wire serial communication as follows. See Application Notes for more details of each function beyond the following description.

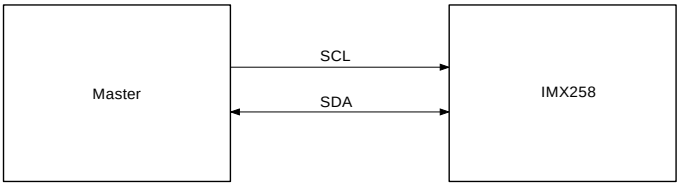


Figure 5 2-wire serial communication

6-2-1 2-wire Serial Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Instance (CCI). CCI is an I2C fast-mode compatible interface, and the data transfer protocol is I2C standard.
This 2-wire serial communication circuit can be used to access the control-registers and status-registers of IMX258-0AMH5-C.

Table 3 Description of 2-wire Serial Communication Pins

pin name	description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of IMX258-0AMH5-C are mapped on the 16-bit address space and the register categories shown as below. Detail register information is shown in Register Map.

Table 4 Specification of register address map for 2-wire serial communication

	address range	description
I^2C register	0x0000 - 0x0fff	Configuration register Read Only and Read/Write Dynamic register
	0x1000 - 0x1fff	Reserved
	0x2000 - 0x2fff	Reserved
	0x3000 - 0xffff	Manufacture specific register

6-2-2 Communication Protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

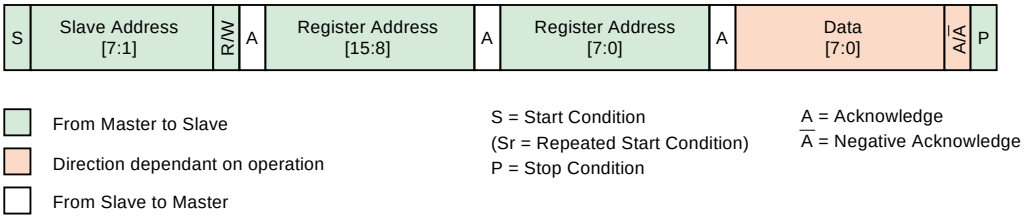
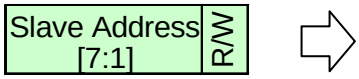


Figure 6 2-wire serial communication protocol

IMX258-0AMH5-C has a default slave address shown as below.
The slave address is selectable by pin connection of SLASEL.
When called by the selected slave address, serial communication interface is activated.
Duplication of the address on the same bus must be prevented.
*For other slave address options, refer to Application Note.



Slave Address (Read or Write) * See Table 5 for R/W bit	SLASEL (pin#43)
MSB 0 0 1 1 0 1 0 R/W LSB	L or NC
MSB 0 0 1 0 0 0 0 R/W LSB	H

R/W shows the direction of communication.

Figure 7 Slave address

Table 5 R/W bit

R/W bit	direction of communication
0	Write (Master → Sensor)
1	Read (Sensor → Master)

6-3 Clock generation and PLL

IMX258-0AMH5-C equips embedded PLL to generate the necessary internal clocks and CSI2 transmission clocks. Set the related registers according to the operation condition. See Application Notes for more details of each function.

6-3-1 Clock System Diagram

IMX258-0AMH5-C is equipped with two PLL, One outputs VTCK for image processing, the other is OPCK for MIPI output.
Based on the clock that is input in the range of 6-27MHz, output of 338-1300MHz can be of the PLL for VTCK, PLL of OPCK for is capable of outputting 338-1300MHz.
It is possible to divide the range of 1/1 to 1/4 of the PLL VTCK, and to multiply in the range of 51-216.
It is possible to divide the range of 1/1 to 1/4 of the PLL OPCK, and to multiply in the range of 51-216.

Typically, IMX258-0AMH5-C can be driven from the dual PLL mode to operate the both of PLLs, but it also supports single PLL mode to move only one side of the PLL.

In PLL single mode, PREPLLCK_IOP_DIV and PLL_IOP_MPY are ignored..

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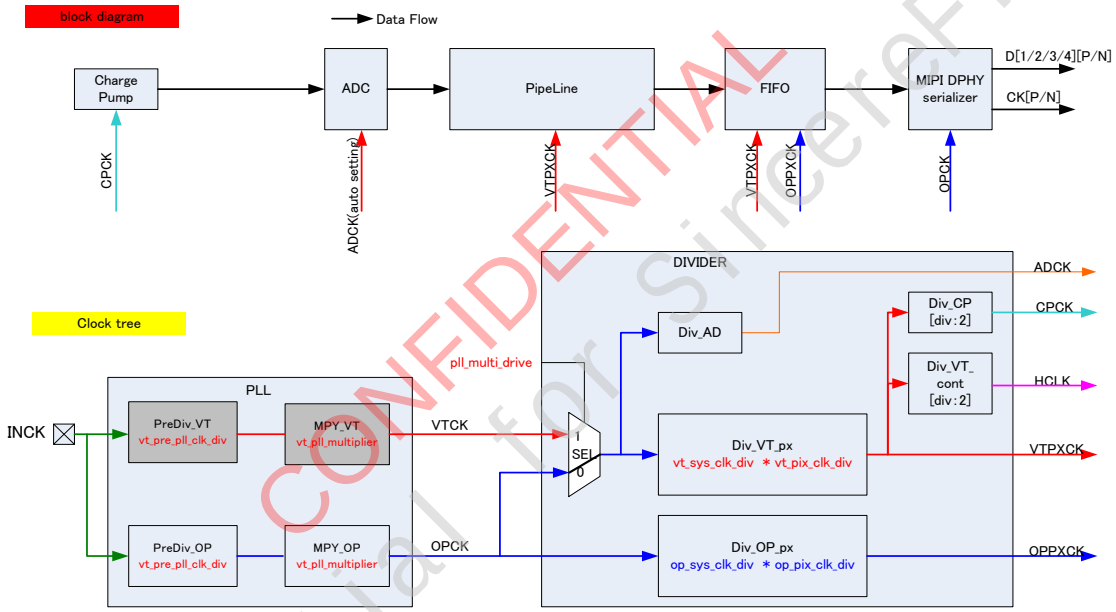

Figure 8 Clock System Diagram (PLL single mode)

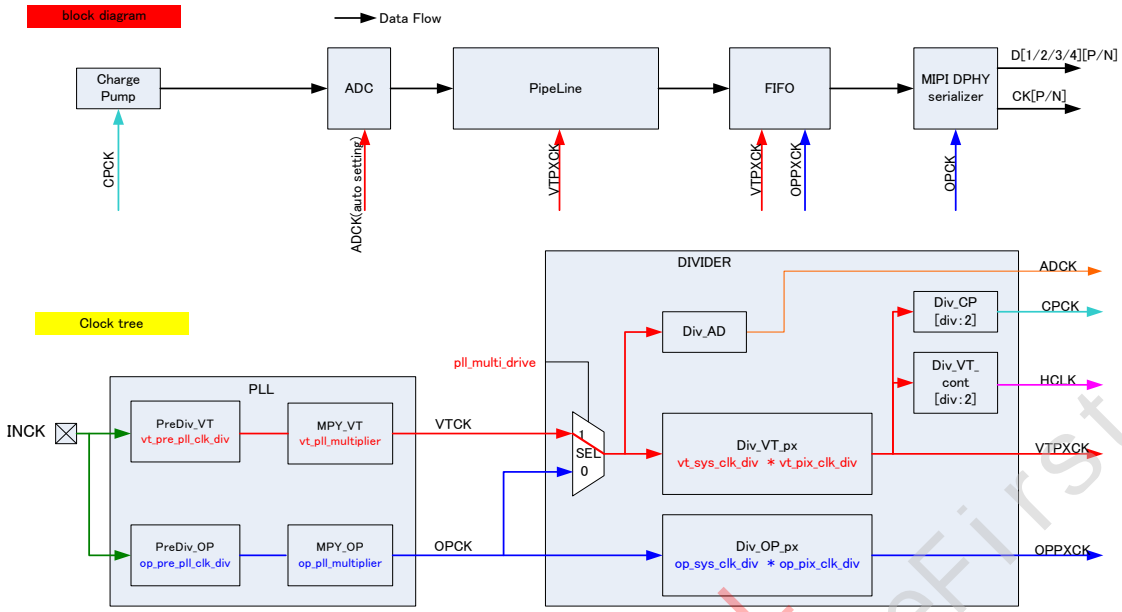

Figure 9 Clock System Diagram (PLL dual mode)

6-4 Description of operation clocks

The followings are general descriptions for each clock. See Application Note for more detail.

6-4-1 INCK

INCK is an external input clock (6 to 27MHz). See “AC characteristics” for electrical requirements to INCK.

6-4-2 VTCK, OPCK(PLL output)

These clocks are the root of all the operation clocks in IMX258-0AMH5-C and it designates the data rate. DCKP/DCKN; CSI2 interface clock is generated from OPCK by dividing into 1/2 (or1/4) frequency since the interface is operated in double data rate format.

6-4-3 VTPXCK Clock

The clock for internal image processing is generated by dividing into 1/10, 1/14, 1/16, 1/20, 1/28, 1/32 or 1/40 frequency. This clock is used as the base of integration time, frame rate, and etc.

6-4-4 OPPXCK Clock

The clock for internal image processing is generated by dividing into 1/8, 1/10, 1/16 or 1/20 frequency according to the word length of the CSI2 interface. This clock is designating the pixel rate and etc.

6-5 Image Readout Operation

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, IMX258-0AMH5-C outputs the image data.

See Application Notes for more details of each function.

6-5-1 Physical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with pin #1 located at the upper left corner.

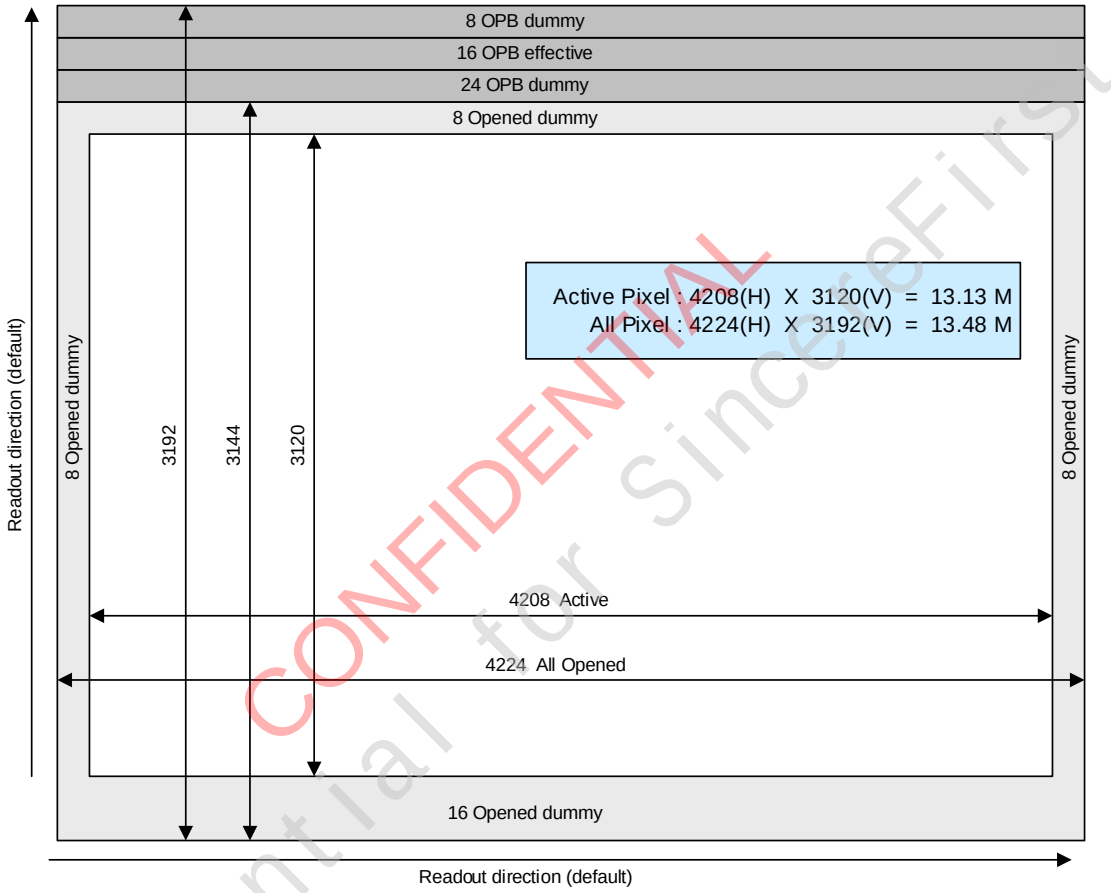

Figure 10 physical alignment of the imaging pixel array

6-6 Output Image Format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.

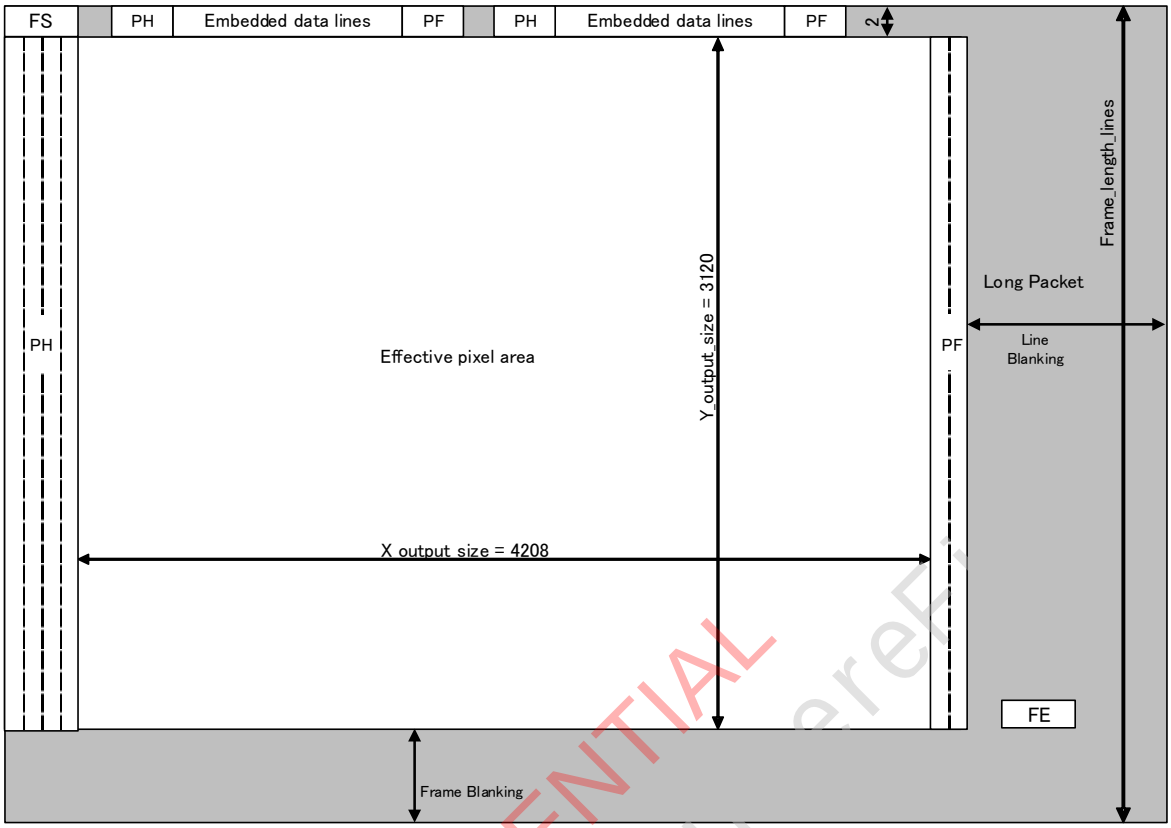

Figure 11 Full pixel output mode data structure

6-6-1 Embedded Data Line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame. The corresponding registers are indicated by “EDL” column of the Register Map.
An unfixed value is output when not outputting embedded data.

See Application Notes for contents and output sequence of Embedded Data Lines.

6-6-2 Image size of mode

IMX258-0AMH5-C can capture and output full size, cropped/scaled image in combination with the normal mode or HDR mode. Examples are shown in the table below. Definitions of each parameter are shown in the below figure.

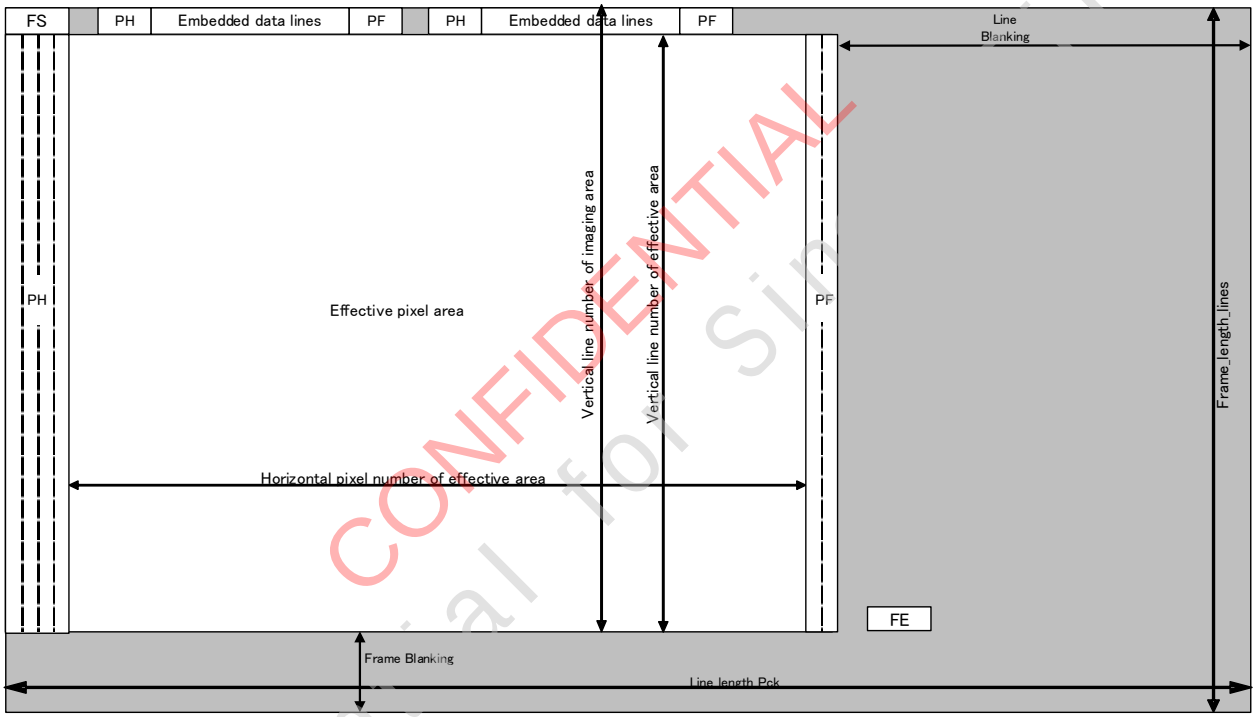

Figure 12 Image size parameter definition

Table 6 modes and image sizes

		Modes							
		Full resolution		2 Sub-sampling / 2 Binning (V: 1/2)		1/3 mode (V: 1/3)		HDR Full-resolution	
Number of vertical lines in imaging area		3121		1561		753		3121	
Number of horizontal pixels in effective area		4208		2100		1400		4208	
Number of lines and start position		Start position	Number of lines	Start position	Number of lines	Start position	Number of lines	Start position	Number of lines
Name of the areas	Frame start	1	1	1	1	1	1	1	1
	Embedded data lines	1	1	1	1	1	1	1	1
	Number of vertical pixels in effective area	2	3120	2	1560	2	752	2	3120
	Frame end	3121	1	1561	1	753	1	3121	1

6-6-3 Description about operation mode

IMX258-0AMH5-C has four modes that All-pixel, Sub-sampling/binning (V:1/2) , binning (V:1/3) and HDR(Full pixel) .

6-6-4 Image area control capabilities

As control function for image's viewing area and /or image size, IMX258-0AMH5-C has capability of analog crop, digital crop, scaling and output crop. The relation of image output size and the resister is shown below.

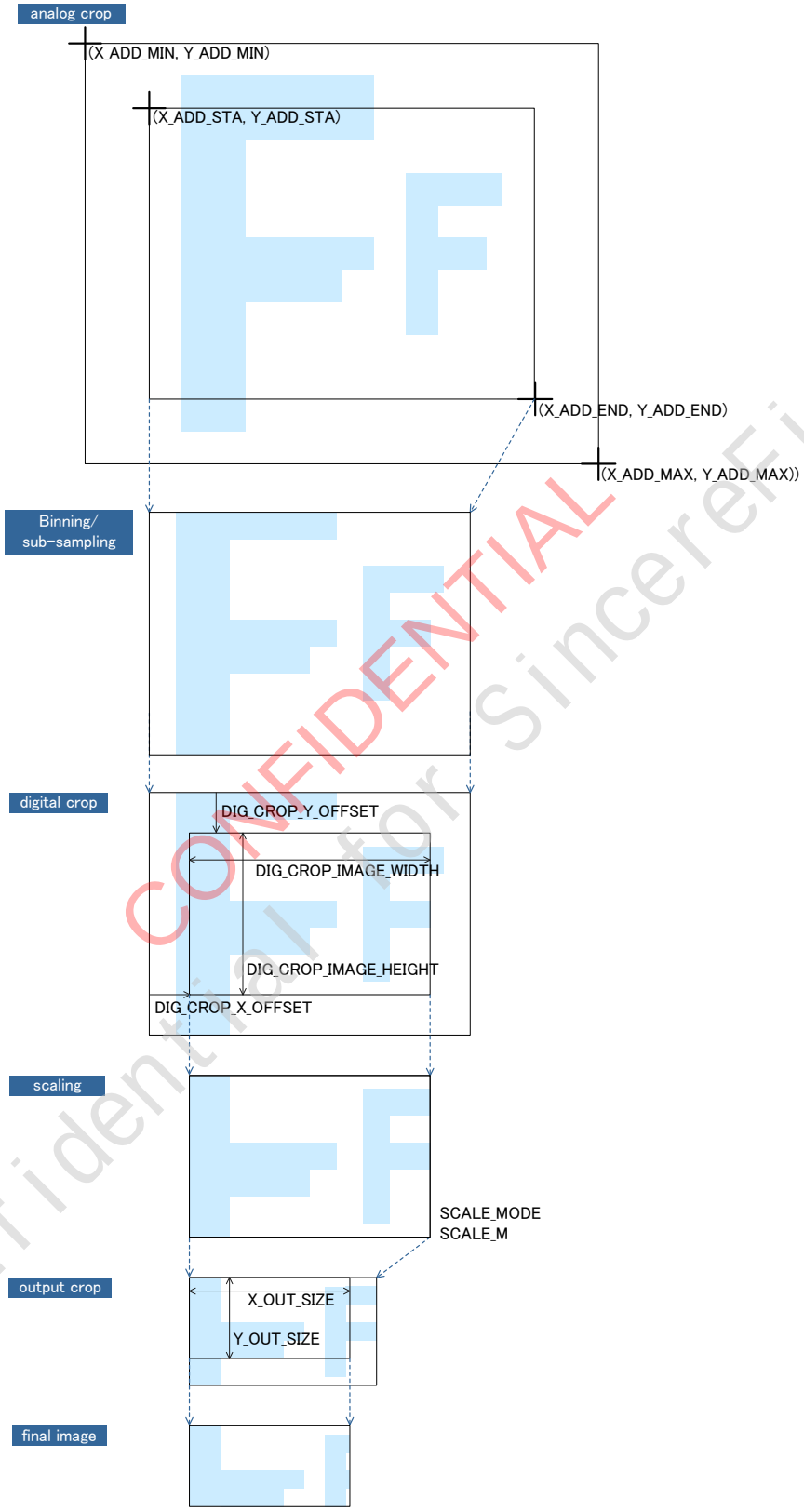

Figure 13 image area control capabilities

Readout Start Position

Default readout position of IMX258-0AMH5-C starts from the lower left when PIN1 is placed at the upper left corner. Because the lens will invert the image both vertically and horizontally, the proper image can be archived when PIN1 is placed at the upper left corner.

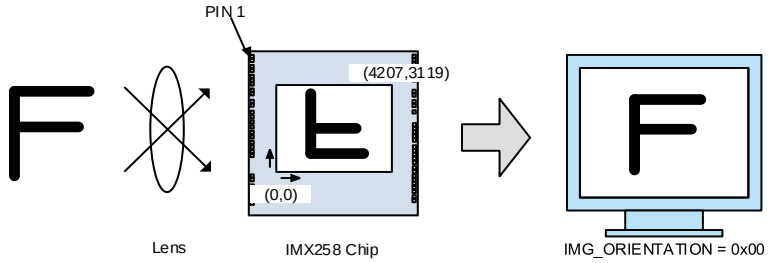

Figure 14 Readout start position

Vertical flip and horizontal mirror readout modes can be specified by the register below. And when readout start and end positions are matching the readout size, the same area is displayed when flipping/mirroring the image. When changing the readout direction, first readout pixel also changes with it.

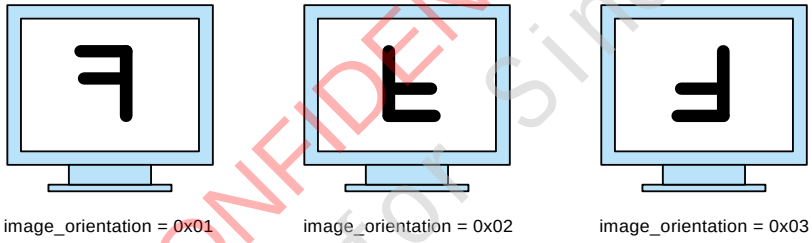

Figure 15 Read out image for each combination of flip and mirror

6-7 Gain setting

IMX258-0AMH5-C can apply analog gain on photo-electron signal and digital gain on digital signal after ADC. Range of settable range is as follows.

Table 7 Range of Gains

	Max.	Note
Analog Gain	24dB	
Digital Gain	24dB	

6-8 Image compensation function

There are some additional functions in sensor image pipeline. Use-case may be chosen in terms of trade-off for power consumption and image quality for example.

See Application Notes for more details of each function.

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6-8-1 Defect Pixel Correction

The defect correction function includes static defect correction and dynamic defect correction.

The static defect correction is to correct the defective pixels according to address data stored in OTP. There is one area for Sony's factory area.
The dynamic defect correction eliminates any critical defects detected on pixel array by estimating from surrounding adjacent pixels value.

6-9 Miscellaneous functions

IMX258-0AMH5-C has the following additional functions to be used for various final products' features.

See Application Notes for more details of each function.

6-9-1 Thermal Meter

This function is to measure the thermal data from internal sensor then average it. Measurement results could be read via I2C or EBD data.

6-9-2 Test pattern output and type of test pattern

IMX258-0AMH5-C can output the following test pattern by build-in pattern generator.
Test pattern of PN9 are available.

6-9-3 Long Exposure Setting

IMX258-0AMH5-C can achieve a very long exposure time (up to 128 times of 1 vertical period) by simply expanding the vertical blanking time setting.

6-9-4 OTP (One Time Programmable Read Only Memory)

Total of 4K bit of OTP is available for users. The area available for the user totals 8 pages. Among these pages, total 80 Byte (addr: 0 to 79) can be used at the user's discretion.
It is also possible to configure most of 8 pages to be usable at the user's discretion, if LSC data and model ID function are not necessary to storage in OTP. See OTP manual for details.

6-9-5 Dual sensor synchronization operation

IMX258-0AMH5-C supports synchronized shooting operation of two image sensors by implementing both slave and master mode for each sensor. To enable this feature, master/slave must be set for each sensor by software control method.

6-9-6 Flash light control sequence

IMX258-0AMH5-C can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins (FSTROBE).

6-9-7 Monitor terminal settings

IMX258-0AMH5-C can output 4 internal signals (H Sync/V Sync/Flash strobe/OIS pulse) via monitor terminals. The monitor terminals mean the following three (3) terminals, such as FSTROBE (41 pin), GPO (42 pin) and XVS (48 pin).

6-10 Image signal interface

6-10-1 MIPI transmitter

IMX258-0AMH5-C outputs image signal by CSI2 high speed serial interface consisted of one pair of clock line and four pairs of data line. See MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) version 1.10.00 and MIPI Alliance Specification for D-PHY version 1.10.00 for details.

Because signal is transmitted by differential pair, impedance (generally 100 Ω) between differential pair near the receiver side during HS mode is required. Otherwise, select receiver with build-in impedance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

7. How to operate IMX258-0AMH5-C

7-1 Power on Reset

IMX258-0AMH5-C does not have the built in “Power On Reset” function.
The XCLR pin is set to “LOW” and the power supplies are brought up. Then the XCLR pin should be set to “High” after INCK supplied.

7-2 Power on sequence

7-2-1 Power on slew rate

Maximum slew rate (mV/us) is specified for each power supply to avoid oscillation during power on.

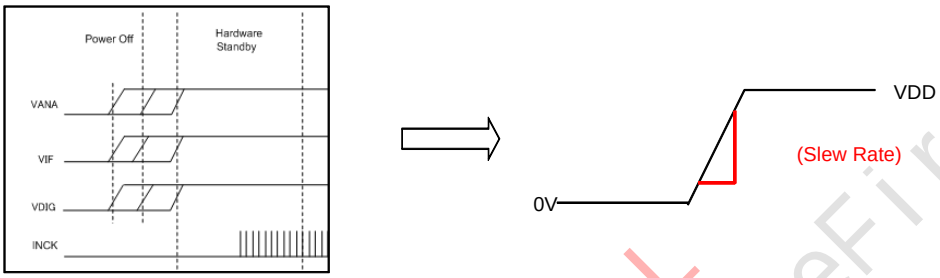

Figure 16 Power on slew rate

Table 8 Limitation on power-on slew rate

Power Supplies	Slew Rate			Comment
	Min	Max	Unit	
VANA, VIF, VDIG		50	mV/μs	

7-2-2 Startup sequence with 2-wire serial communication (external reset)

Follow the power supply start up sequence as below.

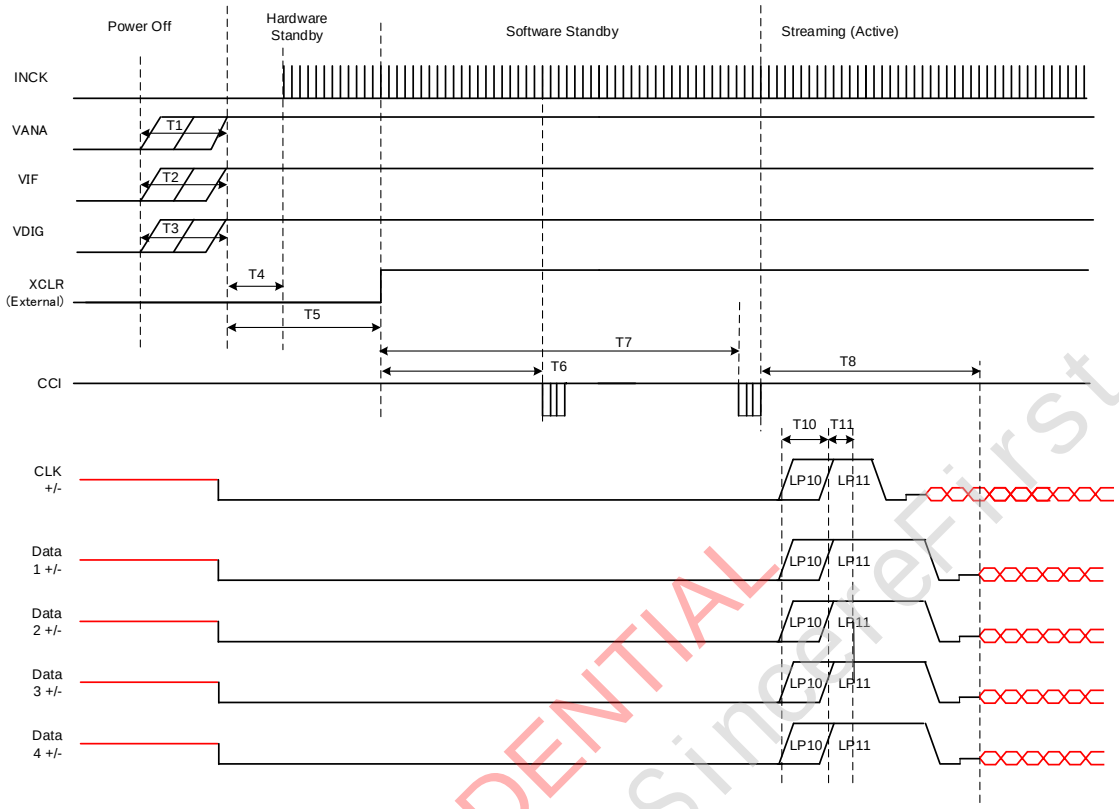

Figure 17 Startup sequence with 2-wire serial communication (external reset)

* Presence of INCK during Power Off is acceptable despite of above chart.

Table 9 Startup sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA ON	T1	VANA and VDIG and VIF may rise in any order.		µs	Slew rate of VANA, VDIG and VIF (0%-100%): Max50 mv/us
VDIG rising – VDIG ON	T2			µs	
VIF rising – VIF ON	T3			µs	
VANA and VDIG and VIF rising - INCK start	T4	0		µs	Presence of INCK during Power off is acceptable
VANA and VDIG and VIF rising - XCLR rising	T5	0		ms	After T1,T2 and T3
INCK start and XCLR rising till CCI Read version ID register wait time	T6	0.4		ms	
INCK start and XCLR rising till Send Streaming Command wait time (To complete reading all parameters from NVM)	T7	12		ms	
Start of first streaming from Sending Streaming Command.	T8		2.0 ms + The delay of the coarse integration time value		
DPHY power up	T10	1	1.1	ms	
DPHY init	T11	100	110	µs	

Note) XCLR needs to be Low until all power supplies complete power-on

7-3 Power down sequence

7-3-1 Power down sequence with 2-wire serial communication (external reset)

Follow the power down sequence below.

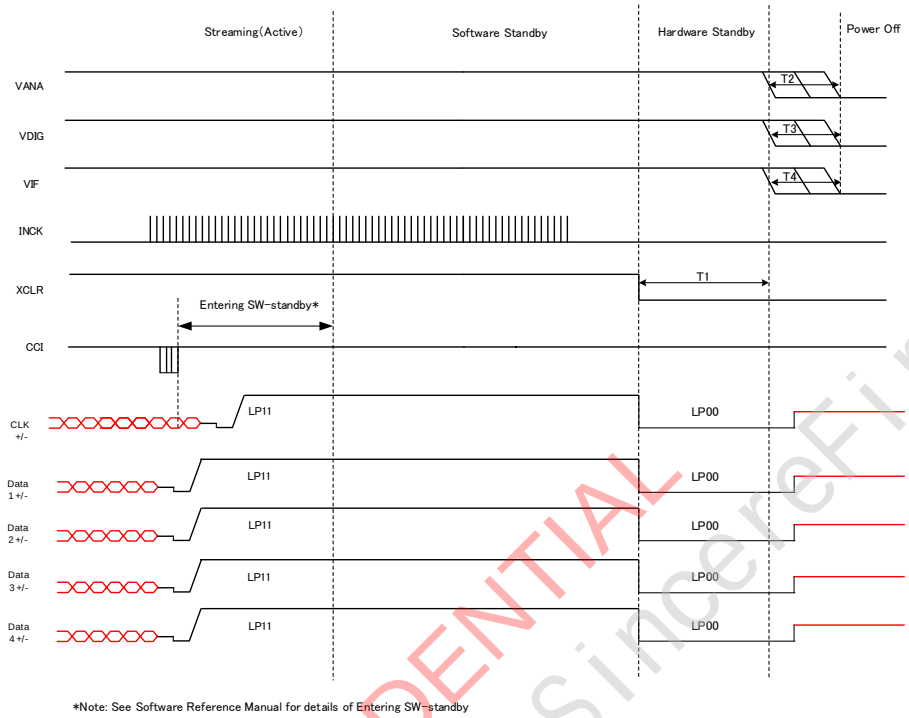

Figure 18 Power down sequence with 2-wire serial communication (external reset)

Table 10 Power down sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
XCLR Neg-edge - VANA (VDIG or VIF) fall	T1	0		µs	Presence of INCK during Power Off is acceptable.
Sequence free of VANA falling and VDIG falling and VIF falling	T2,T3,T4	VANA and VDIG and VIF may fall in any order.		µs	

7-4 Register Map

See Register Map.

8. Electrical Characteristics

The Electrical Characteristics of the IMX258-0AMH5-C is shown below

8-1 DC characteristics

Table 11 DC Characteristics

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VDDSUB VDDHCM1,2 VDDHSN1,2,3 VDDHAN VDDHPL	VANA		2.6	2.7	2.9	V
	VDDLCN1,2 VDDLSC1,2,3,4,5,6 VDDLIO1,2	VDIG		1.1	1.2	1.3	V
	VDDMIO1,2	VIF		1.7	1.8	1.9	V
Digital input voltage	SDA	VIH		0.7VIF		2.9	V
	SCL	VIL		-0.3		0.3VIF	V
Digital input voltage	XCLR INCK SLASEL XVS	VIH		0.65VIF		VIF + 0.3	V
		VIL		-0.3		0.35VIF	V
Digital output voltage	SDA GPO FSTROBE XVS	VOH		VIF-0.4			V
		VOL				0.4	V

8-2 AC Characteristics

8-2-1 Master Clock Waveform Diagram

8-2-1-1 INCK Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK.

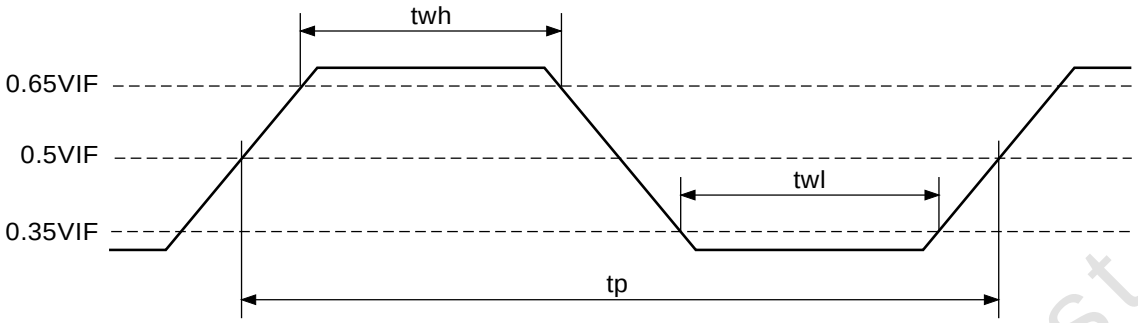

Figure 19 Master Clock Square Waveform Input Diagram

Table 12 Master Clock Square Waveform Input Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{SCK}	6		27	MHz
INCK clock period	t_p	37.0		166.7	ns
INCK low level width	t_{wl}	0.4tp		0.6tp	ns
INCK high level width	t_{wh}	0.4tp		0.6tp	ns
INCK jitter	Tjitter			600	ps

8-2-1-2 INCK Sine Waveform Input Specifications

IMX258-0AMH5-C does not support the “AC coupled connection”.
Therefore, there is no description of AC characteristics

8-2-2 PLL block characteristics

Electrical characteristics of PLL block is shown below.

Table 13 PLL block characteristics (VT system, OP system)

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	6.0		12.0	MHz	
VCO frequency range	338		1300.0	MHz	
Output frequency range	338		1300.0	MHz	
Settling time			1000	µs	

8-2-3 Definition of settling time of PLL block

After start operation, the oscillation frequency of PLL output transits from 0 Hz to target frequency then gradually become stable. The duration for oscillation frequency becomes within 5 % of the target frequency is defined as “settling time”.

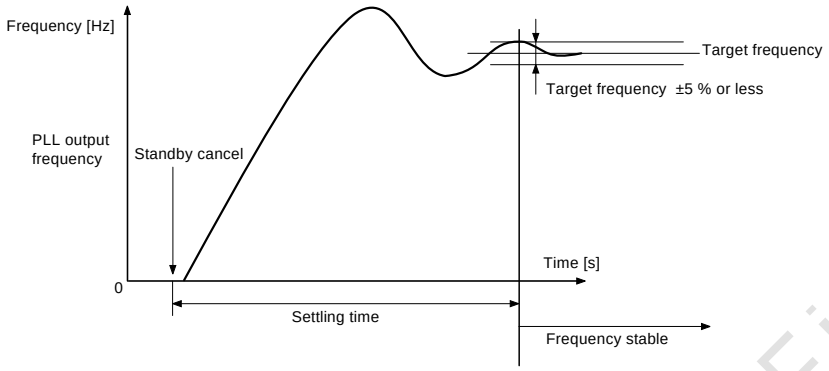

Figure 20 Definition of settling time

8-2-4 2-wire serial communication block characteristics

2-wire serial communication characteristics are shown below.

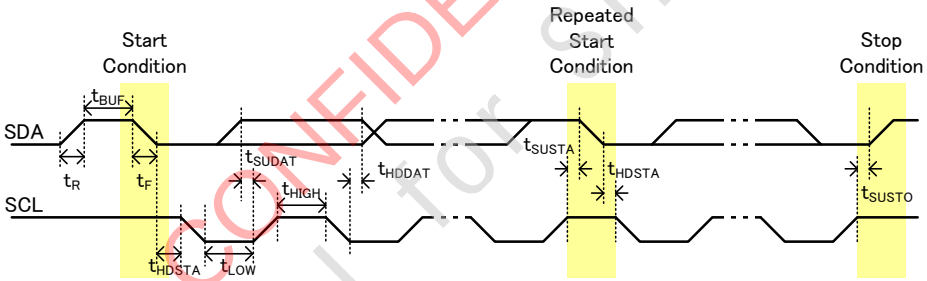

Figure 21 2-wire serial communication block specification

Table 14 2-wire serial communication block specification

Parameter	Symbol	Conditions	Min. (Fast-modePlus)	Max. (Fast-mode Plus)	Unit
Low level input voltage	V_{IL}		-0.3	$0.3V_{IF}$	V
High level input voltage	V_{IH}		$0.7V_{IF}$	2.9	V
Low level output voltage	V_{OL1}	VIF > 2 V, Sink 3 mA	0	0.4	V
	V_{OL2}	VIF < 2 V, Sink 3 mA	0	$0.2V_{IF}$	V
Output fall time	t_{of}	Load 10 pF – 400 pF, 0.7 VIF→0.3 VIF		250 (120)	ns
Input current	I_I	0.1 VIF→0.9 VIF	-10	10	µA
SDA I/O capacitance	$C_{I/O}$			10	pF
SCL Input capacitance	C_I			10	pF

Table 15 2-wire serial communication block AC specification

Parameter	Symbol	Min. (Fast-mode Plus)	Max. (Fast-mode Plus)	Unit
SCL clock frequency	f_{SCL}	0	400 (1000)	kHz
Rise time (SDA and SCL)	t_R	—	300 (120)	ns
Fall time (SDA and SCL)	t_F	—	300 (120)	ns
Hold time (start condition)	t_{HDSTA}	0.6 (0.26)	—	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.6 (0.26)	—	µs
Setup time (stop condition)	t_{SUSTO}	0.6 (0.26)	—	µs
Data setup time	t_{SUDAT}	100 (50)	—	ns
Data hold time	t_{HDDAT}	0	—	µs
Bus free time between Stop and Start condition	t_{BUF}	1.3 (0.5)	—	µs
Low period of the SCL clock	t_{LOW}	1.3 (0.5)	—	µs
High period of the SCL clock	t_{HIGH}	0.6 (0.26)	—	µs

Note) Fast-mode Plus supports only available with INCK ≥ 13.0MHz

8-2-5 Current consumption and standby current

Table 16 Current consumption and standby current

(30 frame/s, V_{ANA} = 2.7 V, V_{DIG} = 1.2 V, V_{IF} = 1.8 V, Tj = 60 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (analog)	I_{ANA}		37.9	43.6	mA	
Current consumption (digital)	I_{DIG}		88.8	130.9	mA	Full-reso, function off
Standby current (analog)	I_{STBANA}			10.0	uA	XCLR : Low fixed INCK :stop
Standby current (digital)	I_{STBDIG}			45.0	mA	XCLR : Low fixed INCK :stop
Standby current (IF)	I_{STBIF}			2.0	uA	XCLR : Low fixed INCK :stop

9. Spectral Sensitivity Characteristic

(Includes neither lens characteristics nor light source characteristics.)

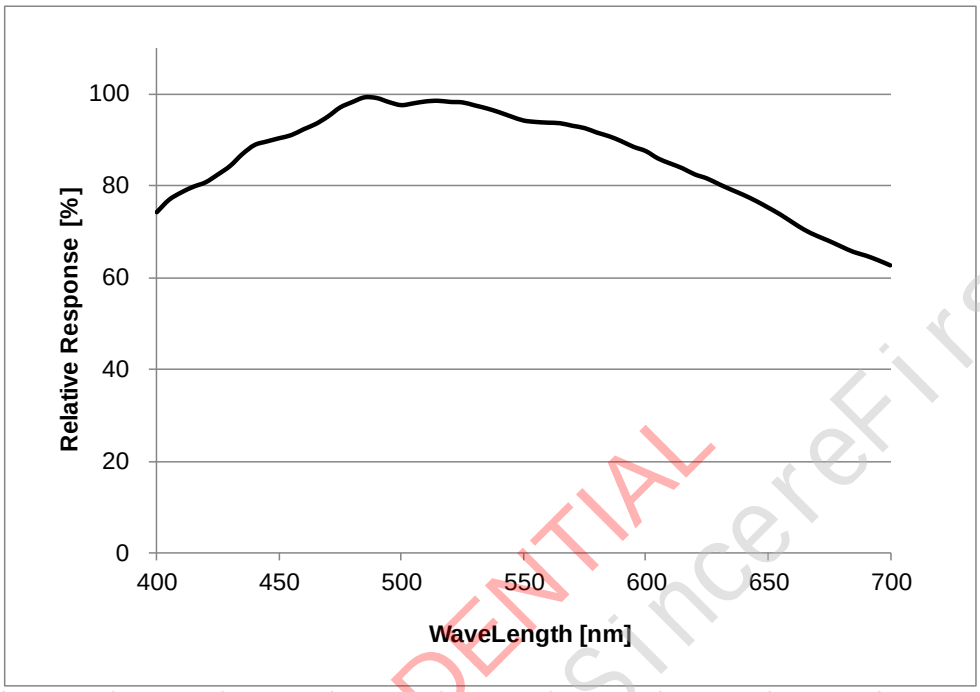

Figure 22 Spectral sensitivity characteristics

10. Image Sensor Characteristics

10-1 Image Sensor Characteristics

Table 17 Image Sensor Characteristics

(30 frame/s, V_{ANA} = 2.7 V, V_{DIG} = 1.2 V, V_{IF} = 1.8 V,Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Range	Measurement method	Remarks
Sensitivity	S	278			LSB	Center	1(*)	1/120 s storage
Saturation signal	Vsat	1023			LSB	Zone1	2(*)	
Video signal shading	SH			70	%	Zone2D	3(*)	Design assurance
Dark signal	Vdt			0.5	LSB	Zone2D	4(*)	When operation at 15 frame/s

(*)These refer to the descriptions of the Measurement Methods on Page 39.

LSB is the abbreviation of Least Significant Bit. 10 bits = 1023 digital is the maximum output code for the output unit. The gain setting (base gain setting) in which the saturation signal output matches with 1023 LSB requires 0[dB] when the OB level is 64 LSB (standard recommended value). The data described at this image sensor characteristics are the measurement standard without base gain setting, and indicates the results evaluated with OB as a reference.

10-2 Zone Definition used for specifying image sensor characteristics

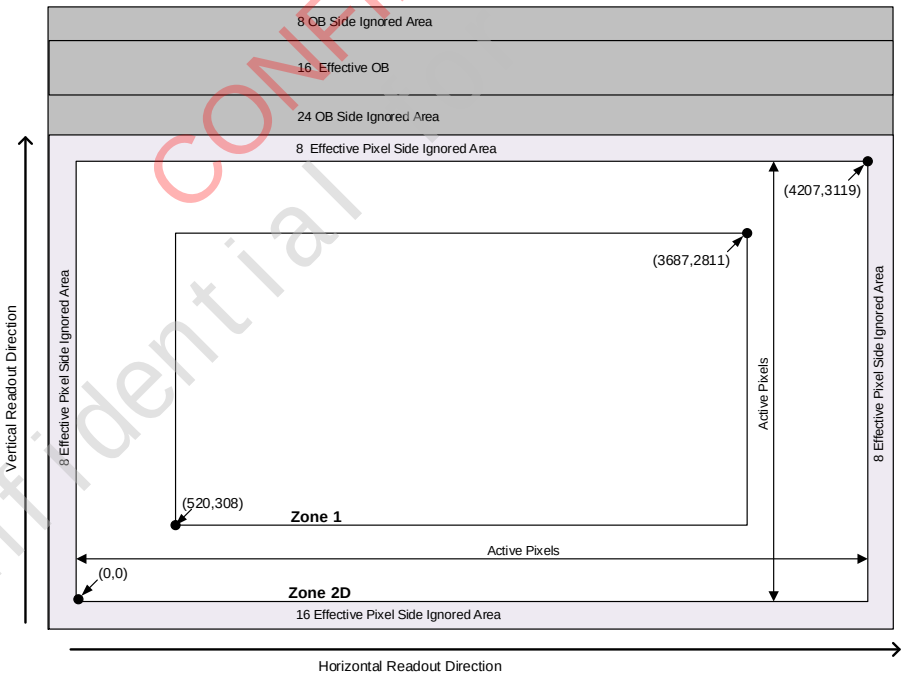

Figure 23 Zone Definition Diagram

11. Measurement Method for Image Sensor Characteristics

11-1 Measurement conditions

The device operation conditions are at the typical values of the bias and clock voltage.

Table 18 Measurement Conditions

Supply voltage	Analog 2.7 V, digital 1.2 V, IF 1.8 V
Clock	INCK 18 MHz

In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the pixel digital signal outputs of the measurement system.
As an example of 1 LSB, the typical value is 1 LSB ≈ 0.374 mV in all-pixel output 10-bit operation mode. The minimum value is 0.343 mV and the maximum value is 0.411 mV.

11-2 Pixel position of This Image Sensor and Readout

This image sensor does not have color filter but we call each pixel with their pixel position like normal Bayer sensor as shown in the figure below.
All pixel signals are output successively in a 1/15 s period.

Figure 24 Pixel position

11-3 Definition of Standard Imaging Conditions

11-3-1 Standard imaging condition I

Use a pattern box (luminance: 706 cd/m2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

11-3-2 Standard imaging condition II

A testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or storage time control by the electronic shutter.

11-3-3 Standard imaging condition III

A recommended testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output or storage time control by the electronic shutter.

11-4 Measurement method

11-4-1 Sensitivity

Set the measurement condition to the standard imaging condition I. After the electronic shutter mode with a shutter speed of 1/300 s, measure the pixel signal outputs (Vpix) at the center of imaging area, and substitute the values into the following formula.

S = {(Vpix) × (300/120)} [LSB]

11-4-2 Saturation signal

Set the measurement condition to the standard imaging condition II. After adjusting the luminous Intensity to 20 times the intensity with the average value of the pixel signal outputs, 367 [LSB], measure the average value of the pixel signal outputs.

11-4-3 Video signal shading

Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the pixel signal outputs is 367 [LSB]. Then measure the maximum value (Vmax [LSB]) and minimum value (Vmin [LSB]) of the signal outputs, and substitute the values into the following formula.

SH = ((Vmax –Vmin) /Vmax) × 100 [%]

11-4-4 Dark signal

Measure the output difference between 1/15 [s] signal output (Va) and 1/15000 or less [s] signal output (Vb) at the device ambient temperature of 60 ˚C and the device in the light-obstructed state, and calculate the signal output at 1/15 [s] storage by them using the following approximate formula. Then, this is Vdt [LSB].

Vdt = (Va – Vb) × (1/15) / (1/15) – (1/15000) ≈ (Va –Vb) [LSB]

12. Spot Pixel Specification

Table 19 Spot Pixel Specifications

(15 frame/s, VANA = 2.7 V, VDIG = 1.2 V, VIF = 1.8 V, Tj = 60 ˚C)

Type of distortion	Level Note 1)	Maximum distorted pixels in each zone		Measurement method	Remarks
		Zone2D	Other		
Black or white pixels at high light	30 % ≤ D	65	No evaluation criteria applied	12-3-1	
White pixels in the dark	28 (LSB) ≤ D	975	No evaluation criteria applied	12-3-2	1/30 storage Note 2)

Note) 1. D...Spot pixel level.
2. Continuous same color position pixels in the horizontal or vertical direction are NG.
3. Defect pixels are measured with all optional image processing features (DPC, HDR) disabled..
4. The maximum quantity pixel counts of 65 for Bright Pixels and 975 for Dark Pixels are total of individual pixels.
5. The analog gain for both the Illuminated and Dark defect conditions is 0dB.
6. The above chart (hereinafter referred to as the “White and Black Pixel Specifications”) is the standard only for sorting image sensor products in this specification book (hereinafter referred to as the “PRODUCTS”) before shipment from a manufacturing factory. Sony Corporation and its distributors (collectively hereinafter referred to as the “Seller”) disclaim and will not assume any liability even if actual number of distorted pixels of the PRODUCTS delivered to you exceeds the maximum number set forth in the White and Black Pixel Specifications. You are solely liable for any claim, damage or liability arising from or in connection with such distorted pixels. If the Seller separately has its own product warranty program for the PRODUCTS (the “Program”), the conditions in this specification book shall prevail over the Program and the Seller shall not assume any liability under the Program to the extent there is contradiction.

12-1 Notice on White Pixels Specifications

After shipment inspection of CMOS image sensors, pixels of CMOS image sensors may be distorted and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels.") Cosmic radiation is one of the causes of White Pixels. Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such distorted pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against White Pixels, such as adoption of automatic compensation systems for White Pixels and establishment of quality assurance standards.
White Pixels may be also caused by alpha radiation, which will be emitted in a process of decay of radioactive isotopes which inevitably exist in the air in minute amounts and may exist in materials or parts of CMOS image sensor devices (e.g. packaging materials, seal glass, wiring materials and IC chips). It is recommended that you should use materials or parts which do not include radioactive isotopes, which are sources of alpha radiation, and consider taking measures, such as adoption of vacuum packaging technologies in order to ensure that the PRODUCTS are not exposed to the air. As the density of radioactive isotopes in the air of the underground space may become thicker than that on the ground, it is highly recommended to ensure the PRODUCTS are not exposed to the air in using or storing the PRODUCTS at the underground space.

[For Your Reference] The Annual number of White Pixels Occurrence Caused by Cosmic Radiation

The data in the below chart shows the estimated annual number of White Pixels occurrence caused by cosmic radiation in a single-story building in Tokyo at an altitude of 0 meters. The data shows estimated number of White Pixels based on records of past field tests calculated taking structures and electrical properties of each device into account. However, the data in the chart is for your reference purpose only, and shall not be construed as part of any CMOS image sensor product specifications which the Seller warrants.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
16 LSB or higher	1.3 pcs
29 LSB or higher	0.8 pcs
70 LSB or higher	0.4 pcs
146 LSB or higher	0.2 pcs
210 LSB or higher	0.2 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the annual number of White Pixels occurrence.

Note 4) As this data does not take occurrence of White Pixels caused by alpha radiation into account, White Pixels are likely to occur at higher value than the rate set forth in such data.

For Your Reference:
The annual number of White Pixels occurrence caused by cosmic radiation at an altitude of 3,000 meters will be from 5 to 10 times higher than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence caused by cosmic radiation in such areas approximately doubles when compared with that in Tokyo.

12-2 Measurement Method for Spot Pixels

Measure under the standard imaging condition II.

12-3 Spot Pixel Pattern Specifications

12-3-1 Black or white pixels at high light

After adjusting the average value of the pixel signal output to 367LSB, measure the local dip point (black pixel at high light, VXB) and peak point (white pixel at high light, VXK) in the pixel signal output Vx , and substitute the values into the following formula.
The 367LSB does not include the dark level offset of 64. The average value is calculated using the signal level output of Zone 2D.

$$D_K(\text{White Pixel level}) = (V_{XK}/\overline{V_X}) \times 100[\%]$$

$$D_B(\text{Black Pixel level}) = (V_{XB}/\overline{V_X}) \times 100[\%]$$

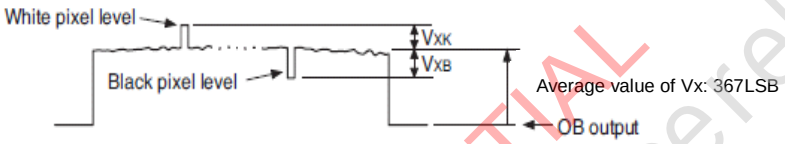

Figure 25 Measurement Method for Spot Pixels

12-3-2 White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

13. CRA Characteristics of Recommended Lens

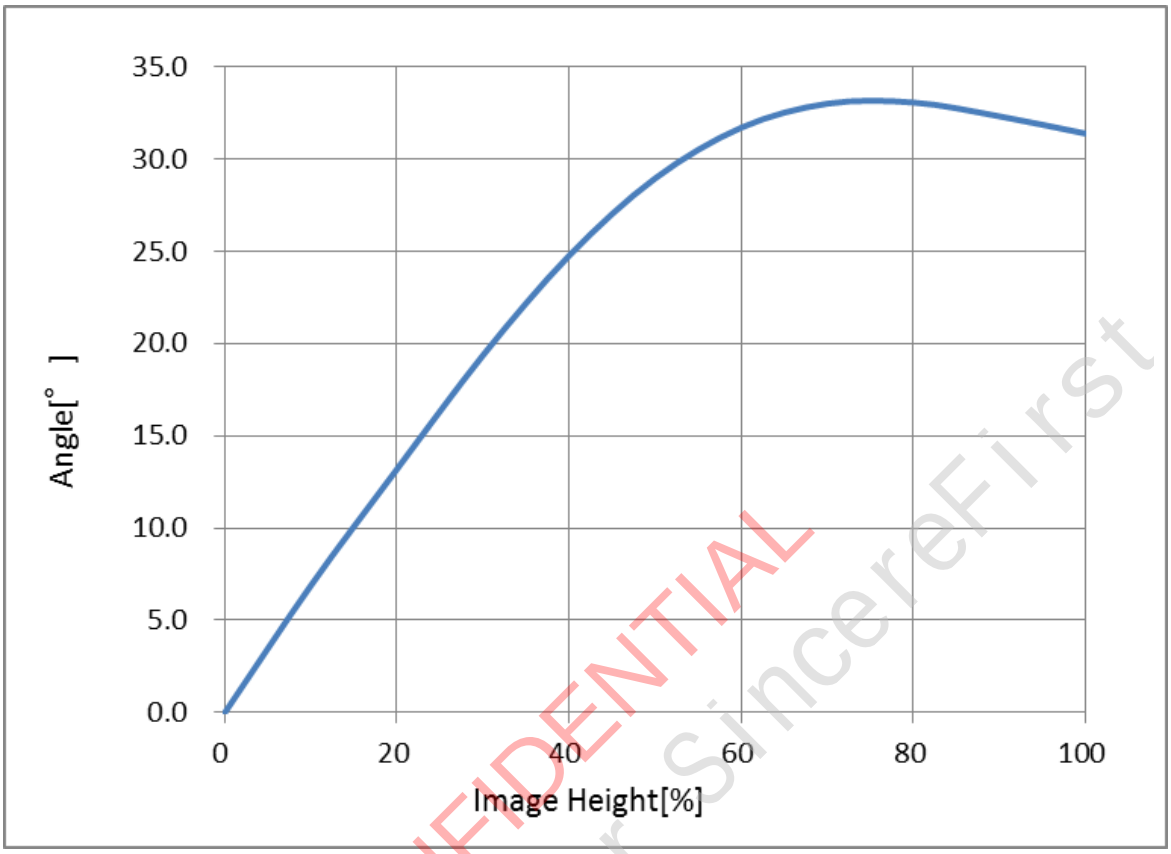

Figure 26 CRA characteristics

14. Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

(1) Perform all work in a clean environment.
(2) Do not touch the chip surface with hand and make any object contact with it.
(3) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

3. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Reliability assurance of this product should be ignored because it is a bare chip.
(5) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(6) Note that X-ray inspection may damage characteristics of the sensor.
(7) Note that the sensor may be damaged when using ultraviolet ray and infrared ray on mounting it.
(8) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

15. Notes on Handling (Additional items concerning bare chip mounting of stacked-type CMOS image sensors)

Collet contact is allowed in areas other than the pixel area, bonding pads, scribe area, and chip edge. Contact with areas other than the contact-allowed area may result in problems such as dust emission or electrostatic breakdown.

Collet contact-prohibited areas

- Pixel area: Abnormal images
- Bonding pad: Circuit electrostatic breakdown
  (Please note that this rule is not applicable for electrostatic breakdown prevention areas.)
- Scribe area: Dust emission due to chipping
- Chip edge: Dust emission due to chip breakage

Note: Ensure sufficient positional accuracy during the pickup work.
Separate the collet contact surfaces and contact-prohibited areas as much as possible.

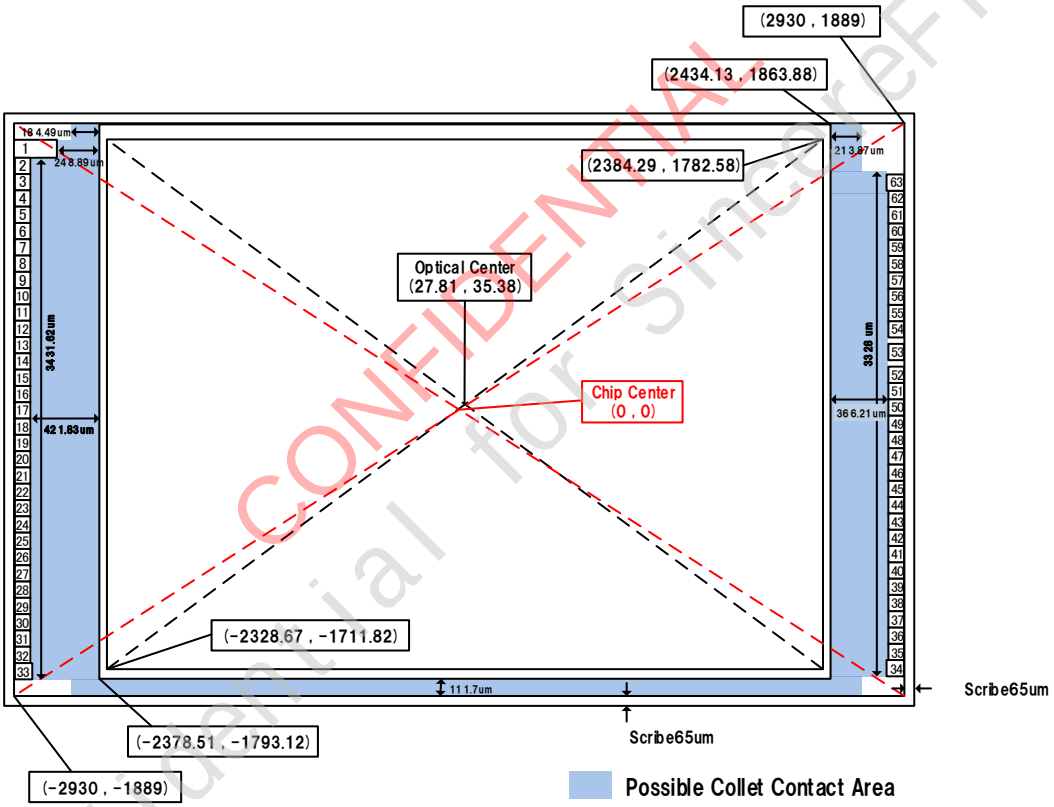

Figure 27 Prohibited Area

Ultrasonic chip clearing is prohibited.
This may result in dust emission from cut surfaces.

16. List of Trademark Logos and Definition Statements

* Exmor RS is a trademark of Sony Corporation. The Exmor RS is a Sony's CMOS image sensor with high-resolution, high-performance and compact size by replacing a supporting substrate in Exmor R™ which changed fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type, with layered chips formed signal processing circuits.