GC13A0 COB

1/3.06” 13Mega CMOS Image Sensor

DataSheet

V1.0

2023-05-30

Ordering Information

◆ **GC13A0-WA1NB**

(Colored, 150um, back grinding, reconstructed wafer)

GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	AUTHOR(S)
V1.0	2023-05-30	Document Release	Ali Hu

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List of Glossary

Expression	Description
CRA	Chief Ray Angle
MIPI	Mobile Industry Processor Interface
OTP	One Time Programmable Read Only Memory
ADC	Analog-Digital Converter
DD	Dead Pixel & Defect Correction
PDAF	Phase Detection Auto Focus
Digital Input & Output Voltage	for INCLK, SBCL, SBDA, XSHUTDOWN, FSYNC, IDSEL
Test Temperature	Temperature in which image quality test is operated

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1. Sensor Overview

1.1 General Description

GC13A0 is a high quality 13Mega Bayer pattern CMOS image sensor (CIS) for cellular phone camera application and other products with embedded camera like tablet PC, smart watch, etc. GC13A0 is designed for full-size capturing at 30 frames per second (fps).

GC13A0 has on-chip 10-bit ADC arrays as well as corresponding image signal process functions (static DD, black level calibration, etc.) to achieve high speed image capturing and high quality image.

The total active pixel array size is 4208 x 3120 to meet with the 1/3.06-inch optical format.

GC13A0 is suitable for fast yet low power consumption application with power supply of 2.8V/1.8V/1.2V, which is useful in extending the battery life of cell phones, tablet PCs and a variety of other mobile products.

The CIS provides RAW10 data format through MIPI interface and can be controlled through camera control interface (CCI).

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1.2 Block Diagram

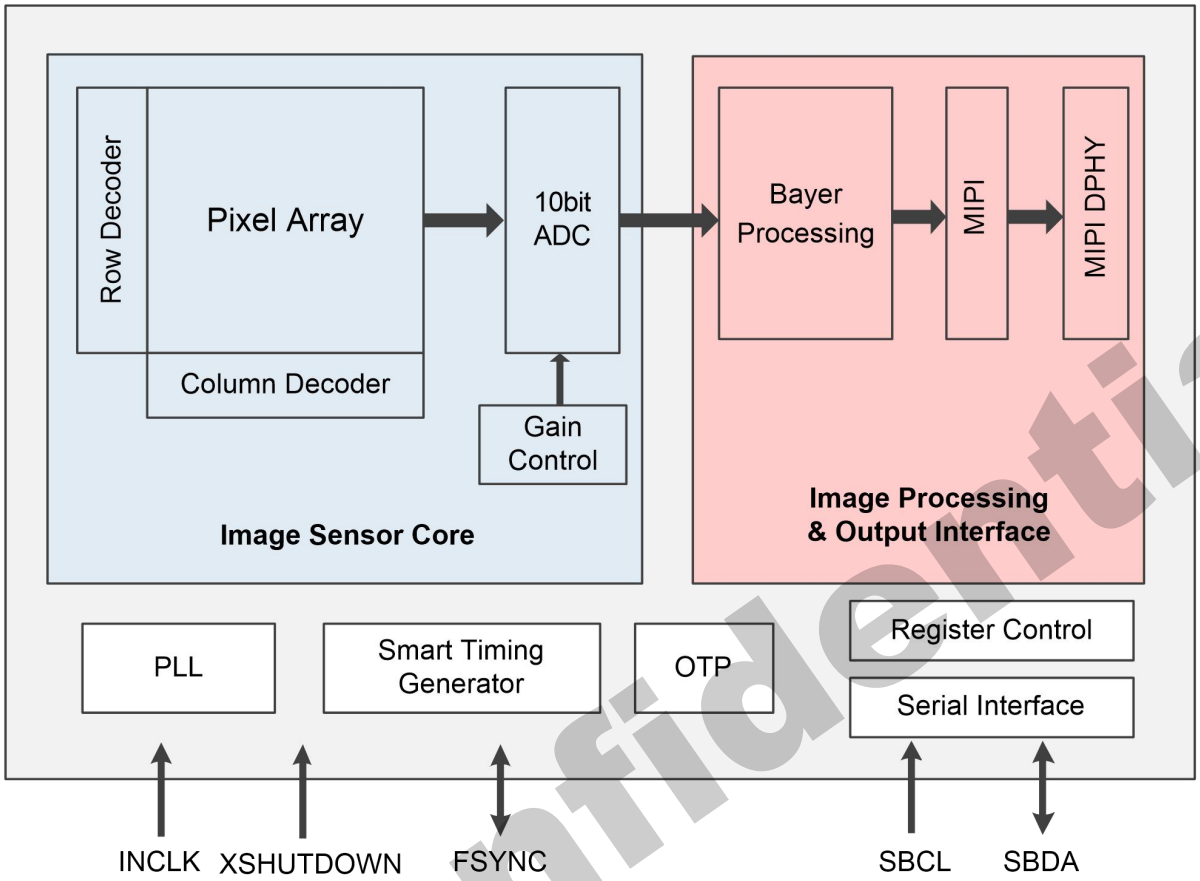

Figure 1- 1 Block Diagram

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1.3 Features

- Optical format : 1/3.06 inch
- Pixel size : 1.12μm x 1.12μm BSI
- Active image size : 4208 x 3120
- Color filter : RGB Bayer Pattern
- Output formats : Raw 10
- Shutter type : Electronic rolling shutter
- Max. full-resolution frame rate : 30fps @13Mp
- Max. video frame rate : 60fps @FHD, 120fps @HD
- MIPI data rate : Max. 1400Mbps/lane
- Lane number : 4-lane @13Mp
  4-lane @HD
- ADC Accuracy : 10 bits
- Power supply requirement : 2.70~3.00V for AVDD (Typical 2.80V)
  1.15~1.30V for DVDD (Typical 1.20V)
  1.15~1.25V / 1.70~1.90V for IOVDD
  (Typical 1.20V / 1.80V)
- Image Flip : Horizontal/Vertical mirror
- Operation temperature : -20℃ ~ 70℃
- Analog Gain : Max. 16x
- OTP support : 8K bits, only for GC
- Package : COB
- Max. optical lens CRA : 33.98
- PDAF : Support PDAF type 3
- PLL support
- Windowing support
- Dual sync application support (master/slave)

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2. Electrical Characteristics

2.1 Absolute Maximum Rating

Table 2- 1 Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit	Note
Analog power supply	V_{AVDD_MAX}	-0.3	-	3.9	V	Refer to GND level
Digital power supply	V_{DVDD_MAX}	-0.3	-	1.8	V	
I/O power supply	V_{IOVDD_MAX}	-0.3	-	3.6	V	
Digital input voltage	V_{I_MAX}	-0.3	-	V_{IOVDD}+0.3	V	
Digital output voltage	V_{O_MAX}	-0.3	-	V_{IOVDD}+0.3	V	
Storage temperature	T_{STR}	-40	-	85	℃	

2.2 Operating Conditions

Table 2- 2 Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit
Analog power supply	V_{AVDD}	2.7	2.8	3.0	V
Digital power supply	V_{DVDD}	1.15	1.2	1.3	V
I/O power supply	V_{IOVDD}	1.7/1.15	1.8/1.2	1.9/1.25	V
Digital input voltage	V_I	0	-	V_{IOVDD}	V
Digital output voltage	V_O	0	-	V_{IOVDD}	V
Test temperature	T_{TEST}	21	25	27	℃
Operating temperature	T_{OPR}	-20	-	70	℃
Performance temperature	T_{SEPC}	0	-	60	℃

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2.3 DC Characteristics

Table 2- 3 DC Characteristics

Items	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}	-	0.7 x V_{IOVDD}	-	-	V
	V_{IL}	-	-	-	0.3 x V_{IOVDD}	V
Input leakage current	I_{IL}	V_{IN} = V_{IOVDD} or VSS	-10	-	10	μA
High level output voltage	V_{OH}	I_{OH} = -100μA	0.7 x V_{IOVDD}	-	-	V
Low level output voltage	V_{OL}	I_{OL} = 100μA	-	-	0.3 x V_{IOVDD}	V
High-z output leakage current	I_{OZ}	V_{OUT} = V_{DVDD} or VSS	-10	-	10	μA

Note:

1. High-z output is applied to SBDA, SBCL & MIPI pins when in High-z state.

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2.4 Input Clock Square Waveform Specifications

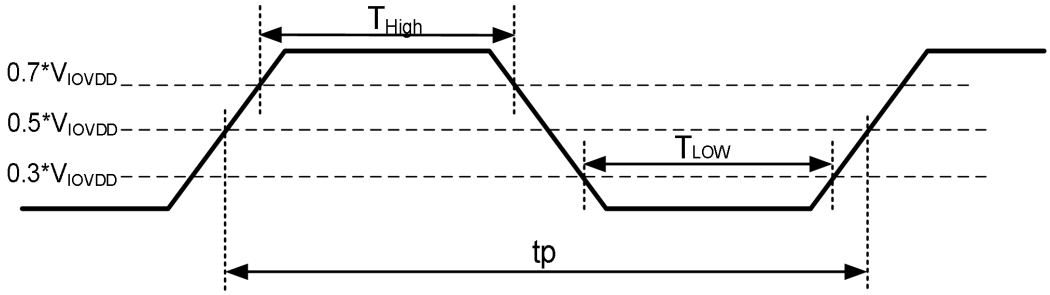

Figure 2- 1 INCLK Wave Diagram

INCLK is the input clock to sensor. Table 2-4 shows some detailed parameters of INCLK square waveform specifications.

Table 2- 4 INCLK Square Waveform Specifications

Item	Symbol	Min.	Typ.	Max	Unit
INCLK Frequency	f_{INCLK}	12	24	27	MHz
INCLK jitter (period, peak-to-peak)	T_{jitter}			600	ps
INCLK high level width	T_{HIGH}	0.4tp		0.6tp	ns
INCLK low level width	T_{LOW}	0.4tp		0.6tp	ns
INCLK period	tp	37.0		83.3	ns
INCLK duty cycle	R_{DUTY}	40		60	%

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2.5 Power Consumption

Table 2- 5 Power Consumption

Item	Symbol	Min	Typ	Max	Unit
4208x3120 @30fps	I_{AVDD}	-	35	45	mA
	I_{DVDD}	-	85	115	mA
	I_{IOVDD}	-	2.2	5	mA
2104x1560 @30fps	I_{AVDD}	-	35	45	mA
	I_{DVDD}	-	68	92	mA
	I_{IOVDD}	-	2.2	5	mA
720p @120fps	I_{AVDD}	-	35	45	mA
	I_{DVDD}	-	55	75	mA
	I_{IOVDD}	-	2.2	5	mA
1080p @60fps	I_{AVDD}	-	35	45	mA
	I_{DVDD}	-	65	88	mA
	I_{IOVDD}	-	2.2	5	mA
Standby current	I_{AVDD}	-	60	200	μA
	I_{DVDD}	-	700	4000	μA
	I_{IOVDD}	-	40	200	μA
Power off current	I_{total}	-		0	μA

Note:

1. All operating current are measured with INCLK running at 24MHz.

2. Standby current is measured at XSHUTDOWN = L, INCLK=24MHz.

3. We recommend that power should be turned off when lower power consumption is required.

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3. Pad Configuration

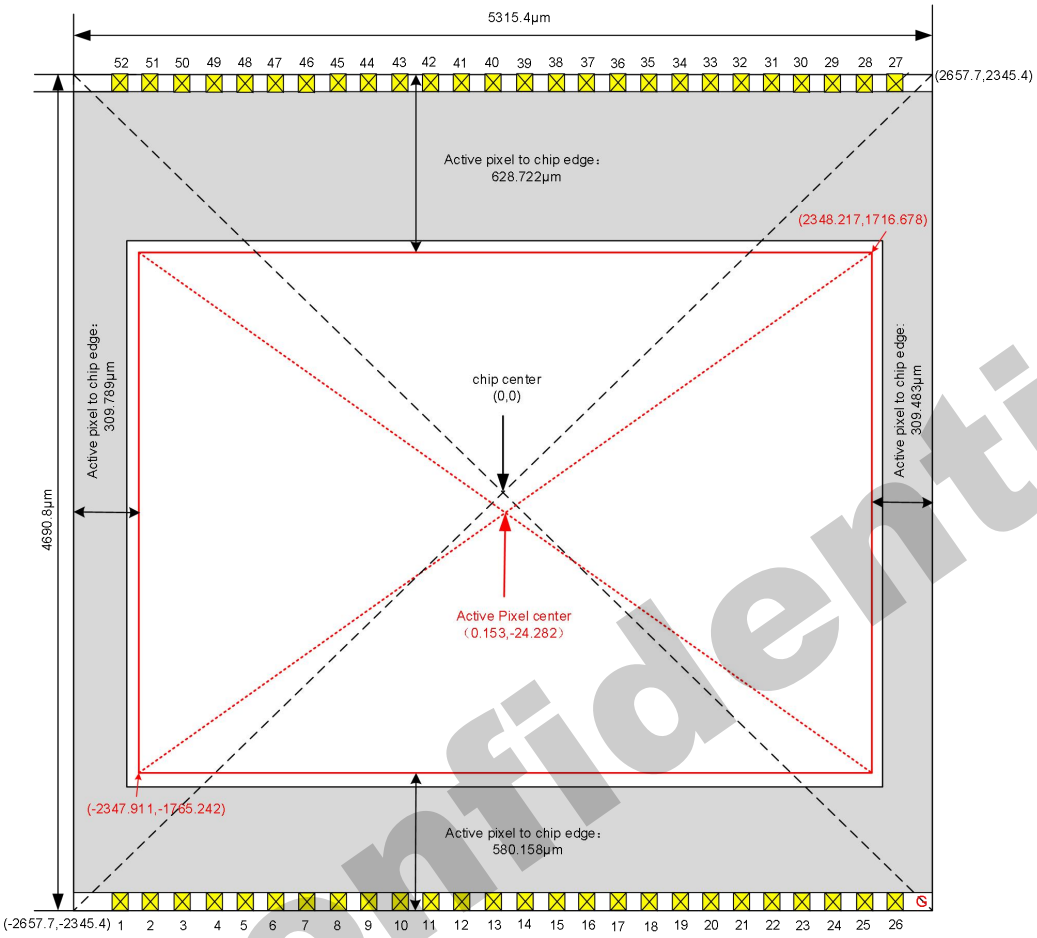

Figure 3- 1 Chip Dimension Top View

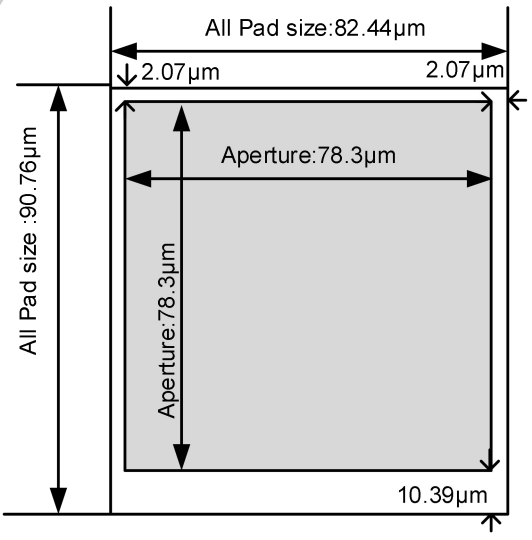

Figure 3- 2 Pad Size and Aperture

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Table 3- 1 Pad Configuration

Die size	• Without Scribe Lane: 5315.4μm x 4690.8μm • With Scribe Lane: 5395.4μm x 4770.8μm
Pad Pitch	189/198/234 μm
Bonding Pad Open size	78.3 μm x 78.3 μm
Total number of pads	52ea
Total number of bonding pads	49ea
Optical Center	(0.153μm , -24.282μm)

3.1 Pad Description

Pin	X-Axis	Y-Axis	Name	Type	A/D	Description
1	-2448	-2252.286	INCLK	input	D	Sensor input clock
2	-2259	-2252.286	PLLVDD	power	D	Internal power supply, connect capacitor to digital ground.
3	-2070	-2252.286	PLLVSS	ground	D	Connect to digital ground.
4	-1872	-2252.286	MDP3	output	D	MIPI data <3> (+)
5	-1674	-2252.286	MDN3	output	D	MIPI data <3> (-)
6	-1476	-2252.286	MDP1	output	D	MIPI data <1> (+)
7	-1278	-2252.286	MDN1	output	D	MIPI data <1> (-)
8	-1080	-2252.286	MGND	ground	D	Ground for MIPI
9	-882	-2252.286	MCP	output	D	MIPI clock (+)
10	-684	-2252.286	MCN	output	D	MIPI clock (-)
11	-486	-2252.286	DVDD12	power	D	Digital power supply pin: 1.2V, connect capacitor to digital ground.
12	-288	-2252.286	MDP0	output	D	MIPI data <0> (+)
13	-90	-2252.286	MDN0	output	D	MIPI data <0> (-)
14	108	-2252.286	MDP2	output	D	MIPI data <2> (+)
15	306	-2252.286	MDN2	output	D	MIPI data <2> (-)
16	504	-2252.286	DVDD12	power	D	Digital power supply pin: 1.2V, connect capacitor to digital ground.
17	693	-2252.286	DGND	ground	D	Ground for digital

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18	882	-2252.286	IOVDD	power	D	Power supply for I/O circuits: 1.8V, connect capacitor to digital ground.
19	1071	-2252.286	IDSEL<1>	input	D	I2C slave address control
20	1260	-2252.286	IDSEL<0>	input	D	I2C slave address control
21	1449	-2252.286	DGND	ground	D	Ground for digital
22	1638	-2252.286	DVDD12	power	D	Digital power supply pin: 1.2V, connect capacitor to digital ground.
23	1827	-2252.286	IOVDD	power	D	Power supply for I/O circuits: 1.8V, connect capacitor to digital ground.
24	2016	-2252.286	DGND	ground	D	Ground for digital
25	2205	-2252.286	DVDD12	power	D	Digital power supply pin: 1.2V, connect capacitor to digital ground.
26	2394	-2252.286	NC	Test pad		No connection pad
27	2326.5	2252.286	AVDD28	power	A	Main power supply pin: 2.8V, connect capacitor to analog ground.
28	2137.5	2252.286	AGND	ground	A	Ground for analog
29	1948.5	2252.286	DVDD12	power	D	power supply pin for digital: 1.2V, connect capacitor to digital ground
30	1759.5	2252.286	DVDD12	power	D	power supply pin for digital: 1.2V, connect capacitor to digital ground
31	1570.5	2252.286	NC	Test pad		No connection pad
32	1381.5	2252.286	NC	Test pad		No connection pad
33	1192.5	2252.286	SGND	ground	D	Connect to digital ground.
34	1003.5	2252.286	SVDD	power	D	power supply pin for digital: 1.2V, connect capacitor to digital ground
35	814.5	2252.286	AVDD28	power	A	Main power supply pin: 2.8V, connect capacitor to analog ground.
36	625.5	2252.286	AGND	ground	A	Ground for analog

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37	391.5	2252.286	XSHUTDOWN	input	D	Chip reset and power down control: 0: chip reset/standby 1: normal work
38	202.5	2252.286	FSYNC	I/O	D	Frame sync control
39	13.5	2252.286	DGND	ground	D	Connect to digital ground.
40	-175.5	2252.286	IOVDD	power	D	Power supply for I/O circuits: 1.8V, connect capacitor to digital ground.
41	-364.5	2252.286	SBDA	I/O	D	Two-wire serial bus, data
42	-553.5	2252.286	SBCL	input	D	Two-wire serial bus, clock
43	-742.5	2252.286	AVDD28	power	A	Main power supply pin: 2.8V, connect capacitor to analog ground.
44	-931.5	2252.286	SVDD	power	D	power supply pin for digital: 1.2V, connect capacitor to digital ground
45	-1120.5	2252.286	SGND	ground	D	Connect to digital ground.
46	-1309.5	2252.286	IOVDD	power	D	Power supply for I/O circuits: 1.8V, connect capacitor to digital ground.
47	-1498.5	2252.286	DGND	ground	D	Ground for digital
48	-1687.5	2252.286	AGND	ground	A	Ground for analog
49	-1876.5	2252.286	AVDD28	power	A	Main power supply pin: 2.8V, connect capacitor to analog ground.
50	-2065.5	2252.286	DVDD12	power	D	Digital power supply pin: 1.2V, connect capacitor to digital ground
51	-2254.5	2252.286	VTX	power	A	Internal power supply, connect capacitor to analog ground.
52	-2443.5	2252.286	VREF	power	A	Internal power supply, connect capacitor to analog ground.

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3.2 Peripheral Circuit Design

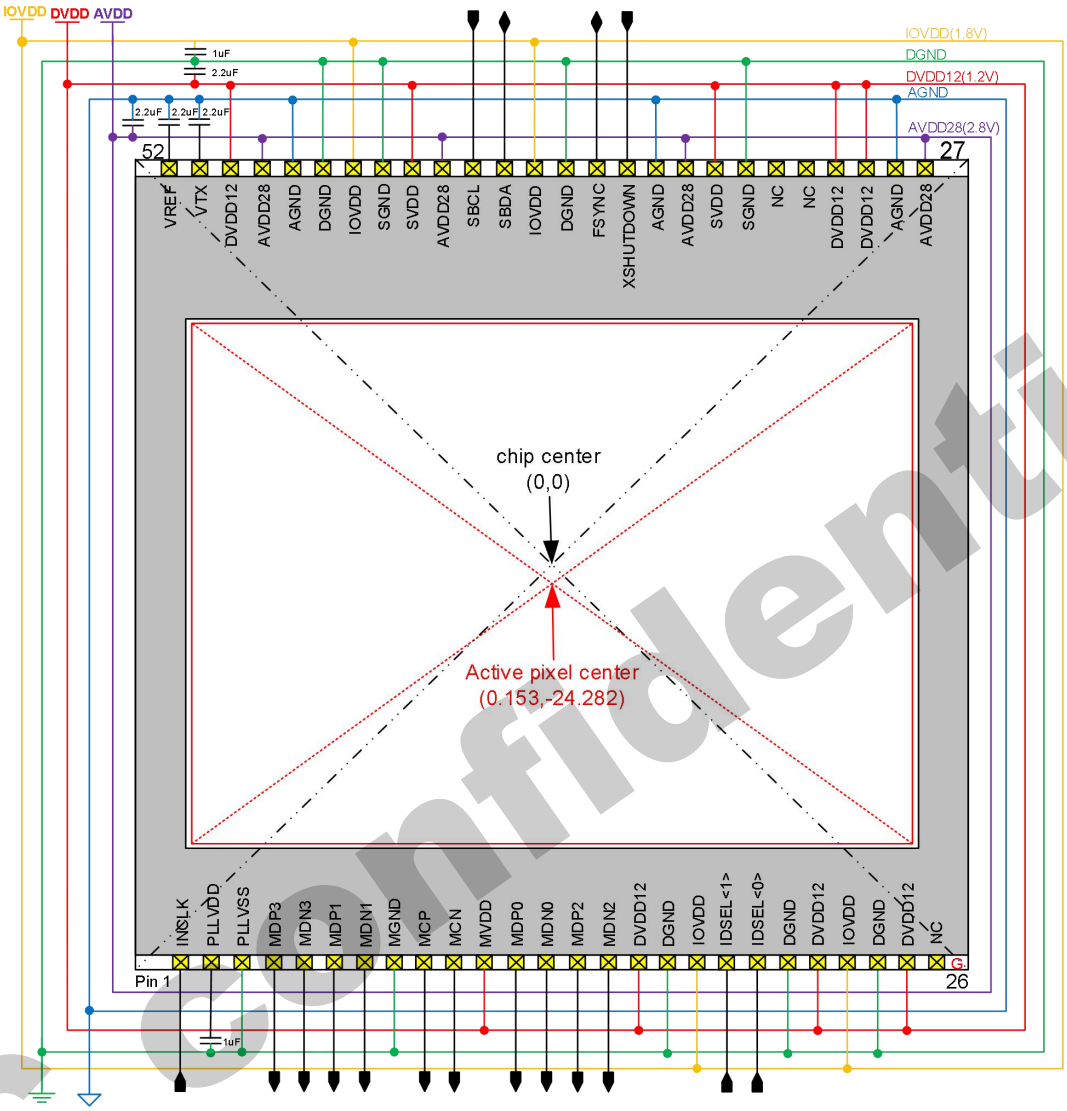

Figure 3- 3 Peripheral Circuit Design

NOTE: DGND & AGND should be maintained separated and connect to each other near the connector

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4. Optical Specifications

4.1 Readout Position

In default status, the first pixel to read out of GC13A0 is located at the lower left corner near pin 1. The image is inverted vertically and horizontally by the lens, which results in a mirrored image output. Readout direction can be set by register 0x0101[1:0].

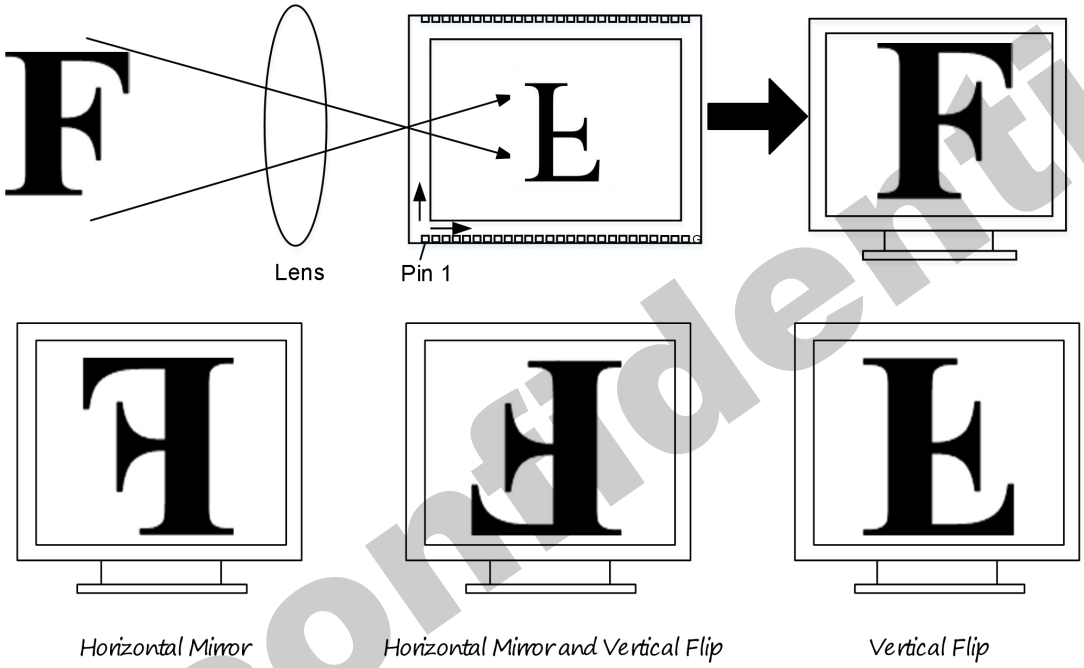

Figure 4- 1 Readout Direction

Function	Register Address	Register Value	First Pixel
Normal	0x0101[1:0]	00	Gr
Horizontal mirror	0x0101[1:0]	01	R
Vertical Flip	0x0101[1:0]	10	B
Horizontal Mirror and Vertical Flip	0x0101[1:0]	11	Gb

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4.2 Pixel Array

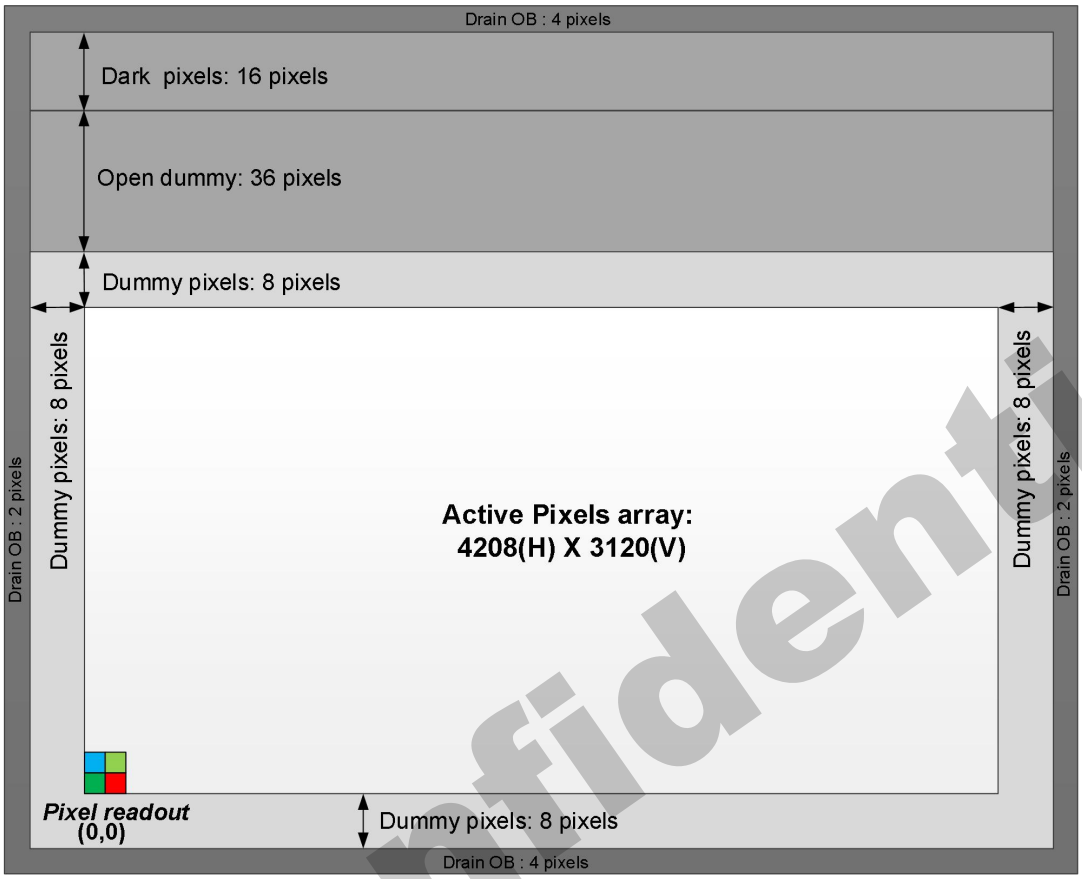

Figure 4- 2 Pixel Array Information

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4.3 Lens Chief Ray Angle (CRA)

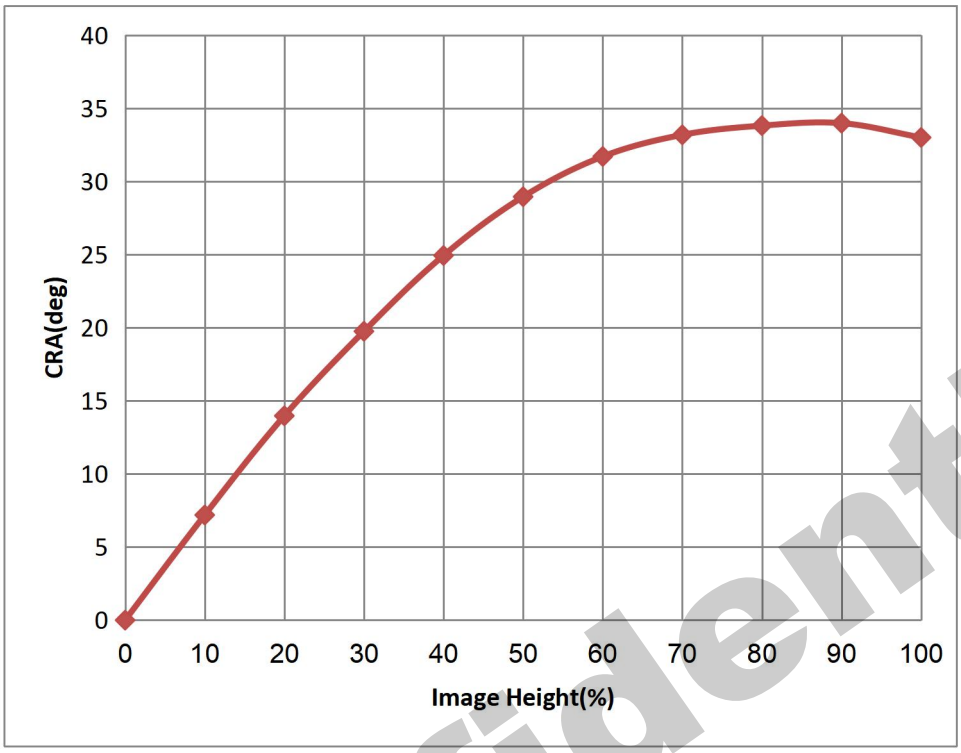

Figure 4- 3 CRA Information

Table 4- 1 CRA Information

Image Height (%)	Image Height (mm)	CRA (degree)
0	0.000	0
10	0.292	7.19
20	0.585	13.97
30	0.877	19.75
40	1.169	24.93
50	1.462	28.95
60	1.754	31.7
70	2.046	33.18
80	2.338	33.81
90	2.631	33.98
100	2.923	33

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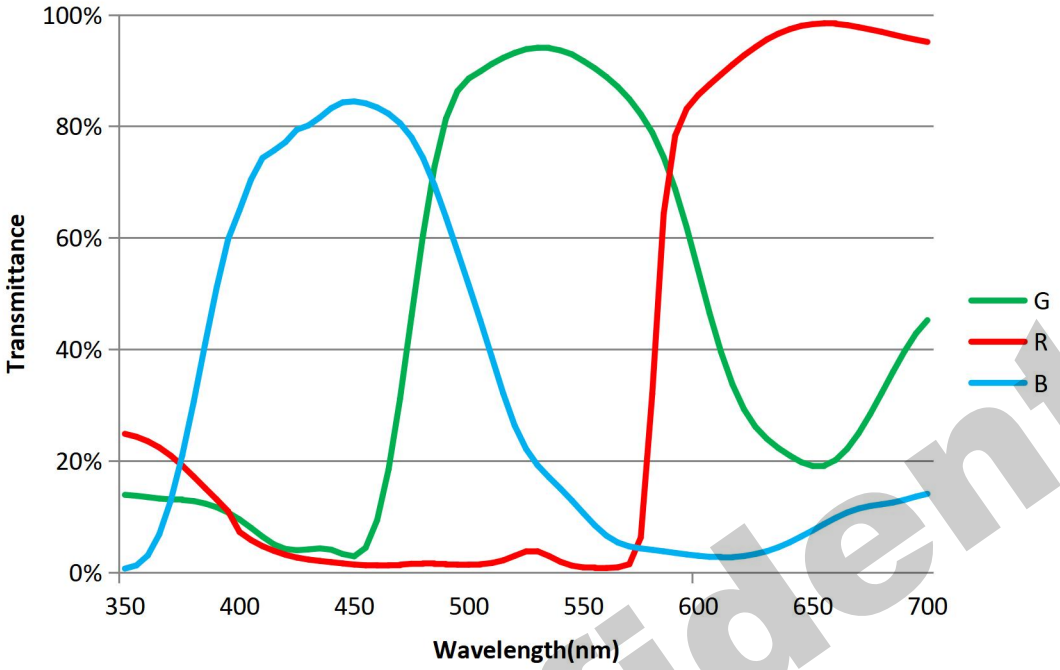
4.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:



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5. Two-wire Serial Bus Communication

In GC13A0 the CCI device ID is controlled by the IDSEL<1:0> pins:

Table 5- 1 Supported Device Address List

IDSEL<1:0>	Slave address write mode	Slave address read mode
00(default)	0x72	0x73
01	0x20	0x21
10	0x22	0x23
11	0x24	0x25

Note: IDSEL<1:0>:1 means connected to IOVDD and 0 means connected to DGND.

5.1 Protocol

The host must perform the role of a communication master and GC13A0 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL.**

There are two kinds of writing operation as well as two kinds of corresponding reading operation, as shown in the following figures.

(a) Writing operation (2 bytes address – 1 byte data)

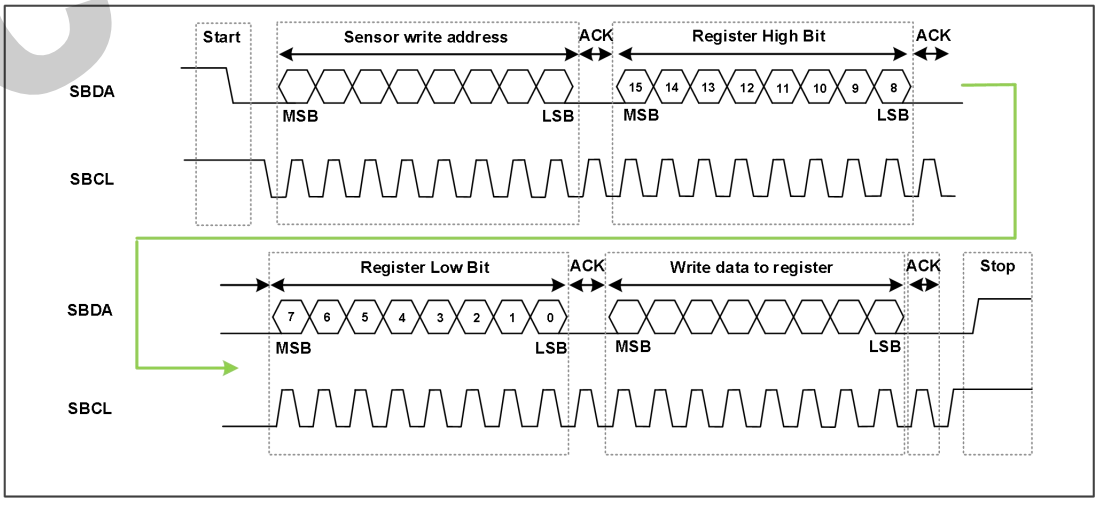

Figure 5- 1 Writing Operation (2 bytes address – 1 byte data)

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(b) Writing operation (2 bytes address – 2 bytes data)

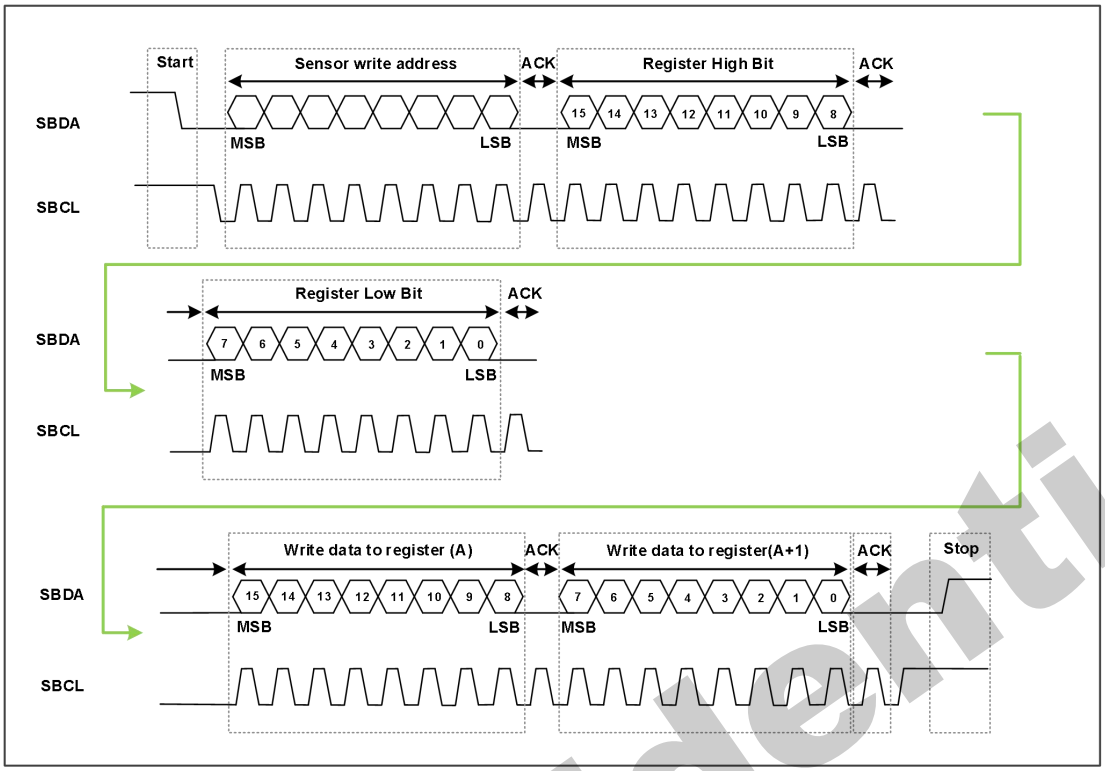

Figure 5- 2 Writing Operation (2 bytes address – 2 bytes data)

(c) Reading Operation (2 bytes address – 1 byte data)

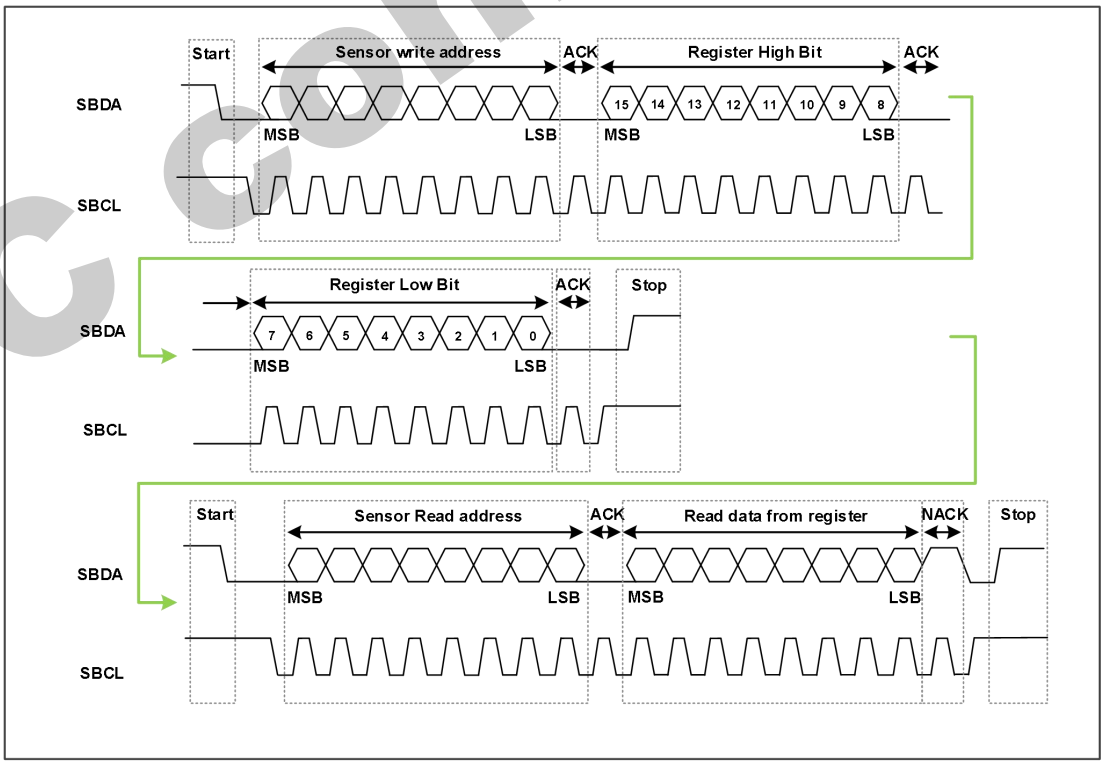

Figure 5- 3 Reading Operation (2 bytes address – 1 byte data)

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(d) Reading Operation (2 bytes address – 2 bytes data)

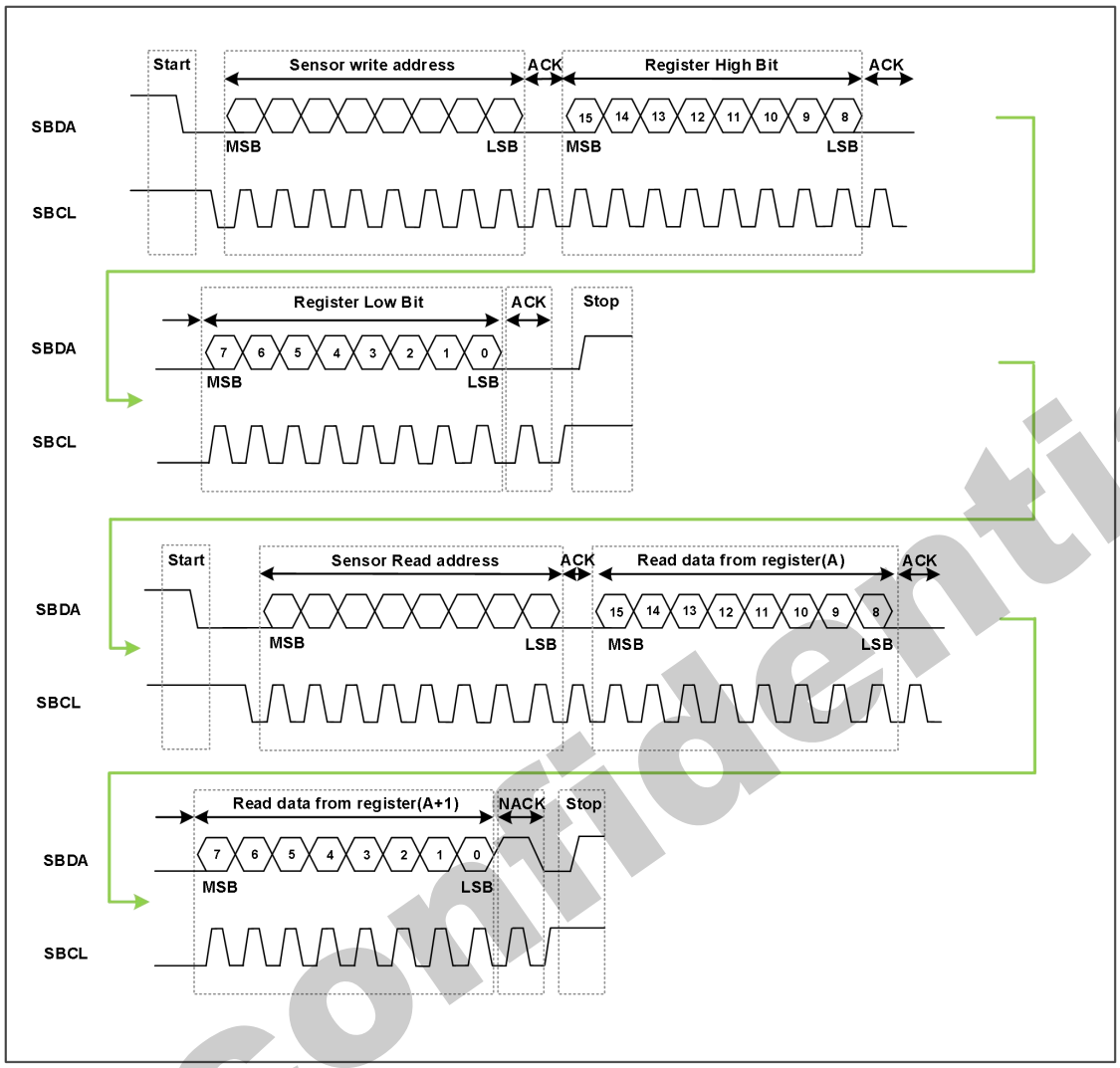

Figure 5- 4 Reading Operation (2 bytes address – 2 bytes data)

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5.2 Serial Bus Timing

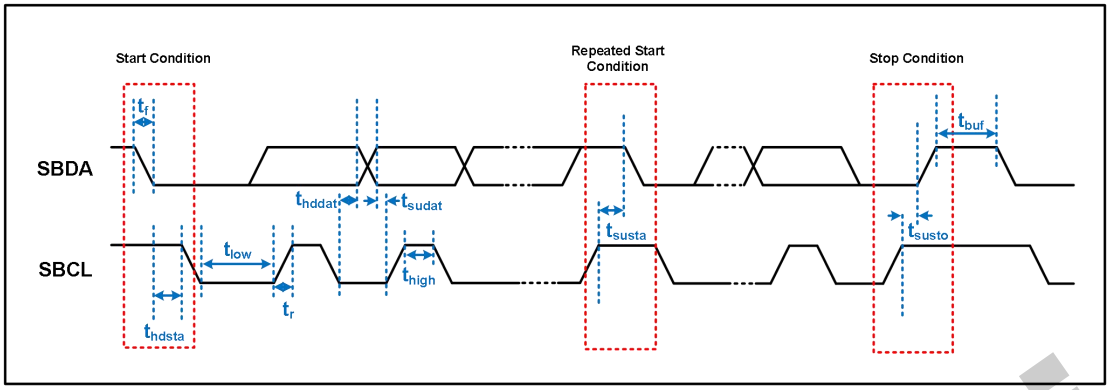

Figure 5- 5 Serial Bus Timing Diagram

Table 5- 2 Two-wire serial communication AC specification: Fast-mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start	t_{buf}	1.3	--	--	μs
Hold time for start condition	t_{hdsta}	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for repeated start condition	t_{susta}	600	--	--	ns
Data hold time	t_{hddat}	0	--	900	ns
Data Set-up time	t_{sudat}	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for stop condition	t_{susto}	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	100	pf

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Table 5- 3 Two-wire serial communication AC specification: Fast-mode plus

Parameter	Symbol	Min	Typ.	Max	Unit
SBCL clock frequency	F_{scl}	0	--	1000	KHz
Bus free time between stop and start	t_{buf}	0.5	--	--	μs
Hold time for start condition	$t_{hd;sta}$	0.26	--	--	μs
LOW period of SBCL	t_{low}	0.5	--	--	μs
HIGH period of SBCL	t_{high}	0.26	--	--	μs
Set-up time for repeated start condition	$t_{su;sta}$	0.26	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	900	ns
Data Set-up time	$t_{su;dat}$	50	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	120	ns
Fall time of SBCL, SBDA	t_f	--	--	120	ns
Set-up time for stop condition	$t_{su;sto}$	0.26	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	550	pf

Note:

1. Fast-mode supports only available with INCLK ≥ 16MHz.

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6. MIPI Transmission

6.1 Clock Lane Low-Power

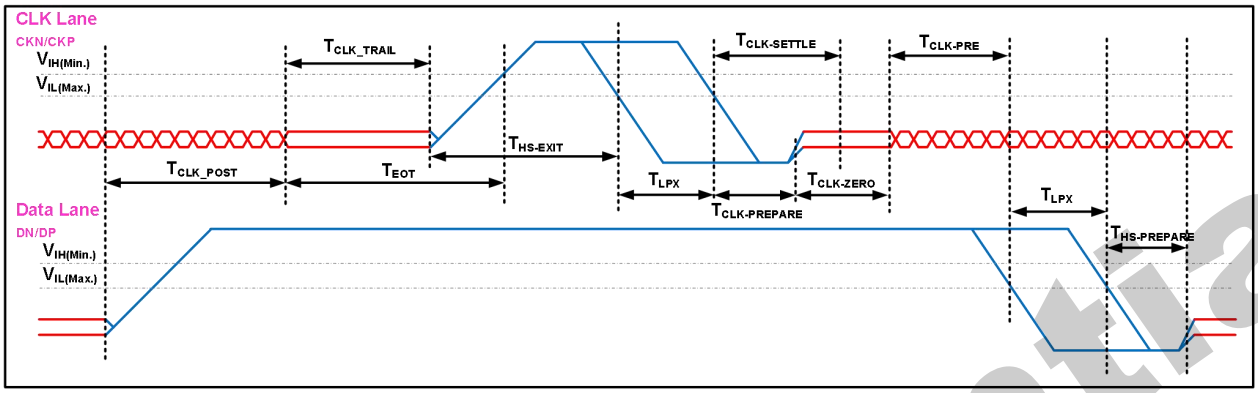

Figure 6- 1 MIPI Clock Lane Diagram

Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only when data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

Table 6-1 shows some detailed register addresses for modifying the clock lane timing.

Table 6- 1 Detailed Register Addresses for MIPI Clock Timing

Register Address	Description
0x0122	$T_{CLK\_HS\_PREPARE}$
0x0123	T_{CLK_ZERO}
0x0124	T_{CLK_PRE}
0x0125	T_{CLK_POST}
0x0126	T_{CLK_TRAIL}

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6.2 HS Data Transmission

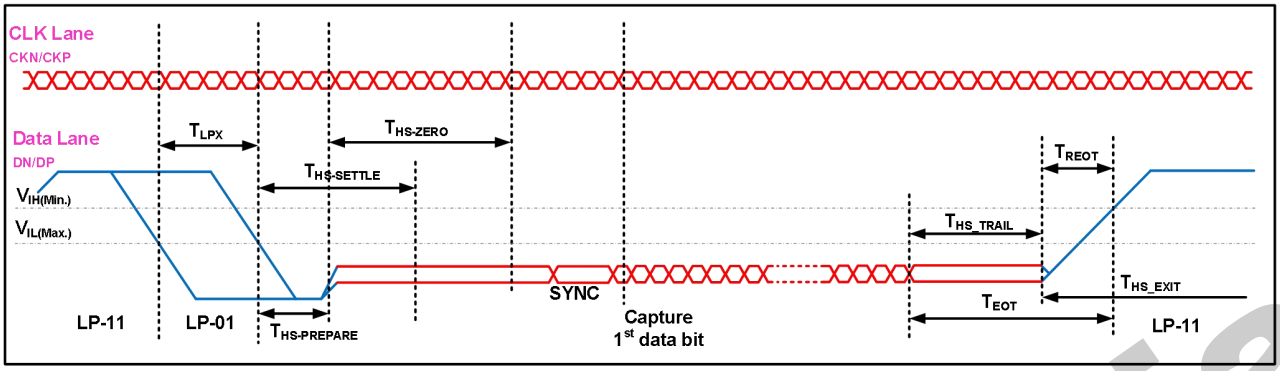

Figure 6- 2 HS Data Transmission

Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

Table 6-2 shows some detailed register addresses for modifying the data lane timing.

Table 6- 2 Detailed Register Addresses for MIPI Data Timing

Register Address	Description
0x0121	T_{LPX}
0x0129	$T_{HS\_PREPARE}$
0x012a	T_{HS_ZERO}
0x012b	T_{HS_TRAIL}
0x0127	T_{HS_EXIT}

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7. Function Description

7.1 Operation mode

The GC13A0 supports three different operating states: Hardware Standby, Software standby, and streaming.

The transition between these states is achieved by issuing proper mode command via the CCI Serial control interface, XSHUTDOWN signal state, and power supplies. Figure 7-1 shows the transition between these states.

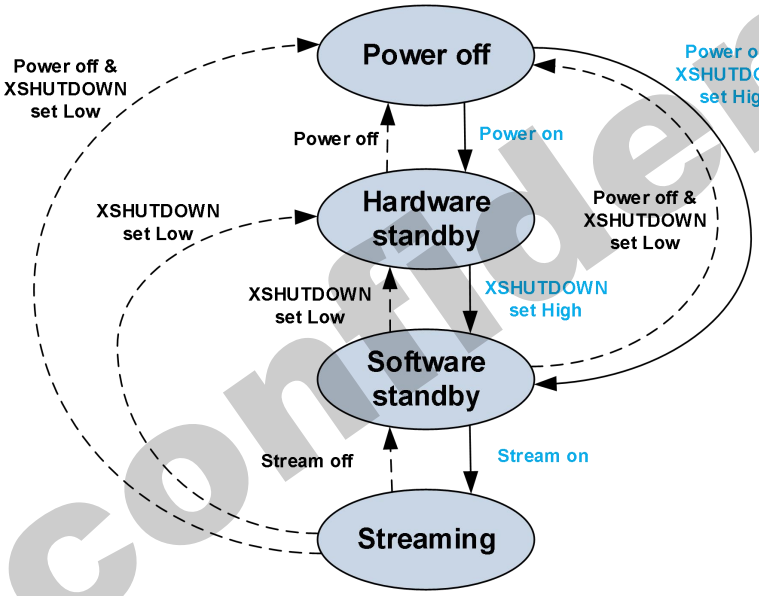

Figure 7- 1 Operation Mode Switching Diagram

Table 7- 1 Detailed Description of Different Operation Mode

Power state	Description	Activate
Power off	Power supplies are turned off	None
Hardware standby	No communication with sensor, low level on XSHUTDOWN	XSHUTDOWN low
Software standby	Two- wire serial communication with sensor, PLL is ready for fast return to streaming mode	Stream mode off XSHUTDOWN high
Streaming	Sensor is fully powered and is streaming image data on the MIPI CSI-2 bus	All

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7.2 Power on Sequence

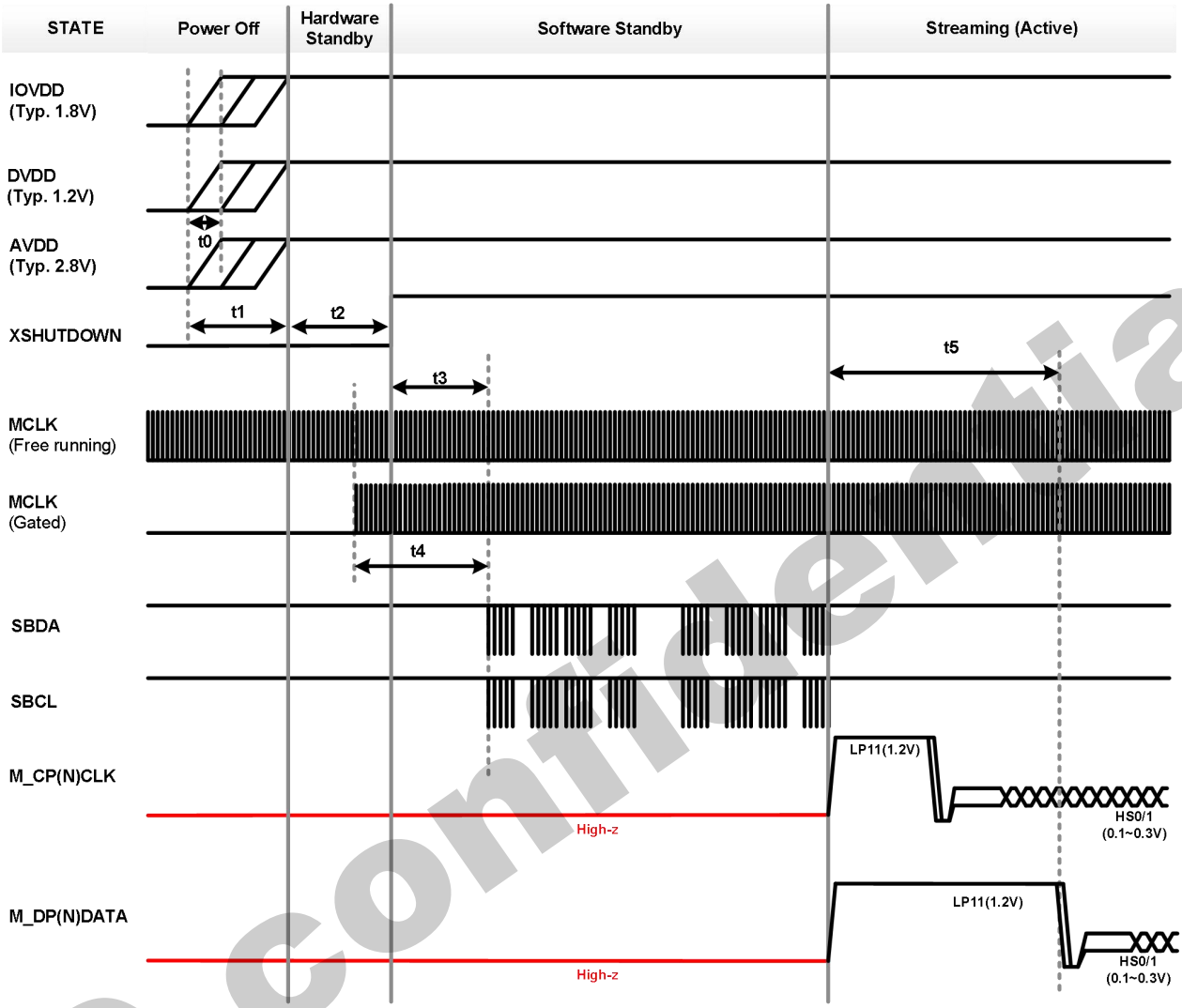

Figure 7- 2 Power on Sequence

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Table 7-2 Detailed Timing Description of Power on Sequence

Parameter	Description	Min.	Max.	Unit
t0	IOVDD/DVDD12/AVDD28 rising time	50	-	μs
t1	IOVDD, DVDD12 and AVDD28 may rise in any order so the rising separation time can vary from 0μs to indefinite	0		μs
t2	From power on to XSHUTDOWN pull high	0	-	μs
t3	From XSHUTDOWN pull high to first I2C transaction	50	-	μs
t4	Minimum No. of MCLK cycles prior to the first I2C transaction	1200	-	MCLK
t5	Entering streaming mode – First frame start sequence	Depend on the setting		ms

Note：

1. IOVDD/DVDD12/AVDD28 may rise in any order. The suggested sequence is IOVDD powered on first, then DVDD12, and AVDD28 last.
2. Register should be reloaded before works.

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7.3 Power off Sequence

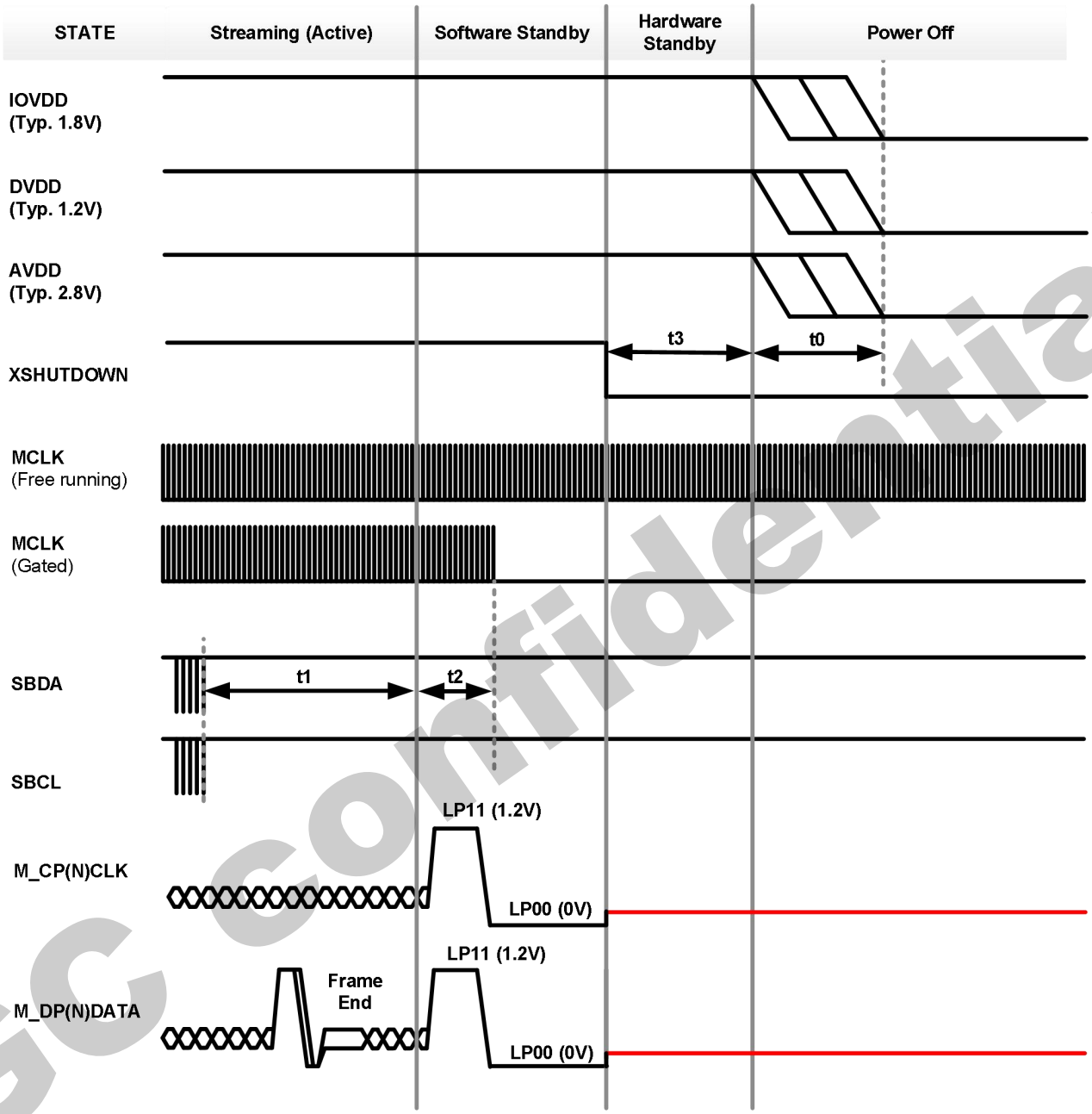

Figure 7- 3 Power off Sequence

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Table 7-3 Detailed Timing Description of Power off Sequence

Parameter	Description	Min.	Max.	Unit
t0	IOVDD, DVDD12 and AVDD28 may pull down in any order, so the falling separation time can vary from 0μs to indefinite	0	-	μs
t1	Enter Software Standby CCI command – Device in Software Standby mode	0	-	μs
t2	Minimum number of MCLK cycles after the last CCI transaction or MIPI frame end code.	2000		MCLK
t3	From XSHUTDOWN pull low to AVDD28/DVDD12 pull down	0	-	μs

Note：

1. IOVDD/DVDD12/AVDD28 may fall in any order. The suggested sequence is DVDD12 and AVDD28 powered off before IOVDD.
2. If the sensor’s power cannot be cut off, please keep power supply, then set XSHUTDOWN pin low. It will make sensor standby.
3. If the standby sequence needs to be modified, please contact FAE of Galaxycore Inc.

7.4 Black Level Calibration

Black level is caused by pixel characteristics and analog channel offset, which makes poor image quality in dark condition and color balance, to reduce these, sensor automatically calibrates the black level every frame with light shield pixel array.

7.5 Integration Time

The integration time is controlled by the integration time registers

Table 7-4 Integration Time Registers

Address	Register name	Description
0x0202	Shutter time	[7:0] shutter time[15:8]
0x0203		[7:0] shutter time[7:0]
0x0340	Frame length	[7:0] frame length[15:8]
0x0341		[7:0] frame length[7:0]

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7.6 Gain Control

GC13A0 supports analog gain and digital gain control through registers, and set separately. The precision of digital gain is 4.10. The analog gain is controlled by register with the precision of 6.10, Analog gain of GC13A0 can be calculated by the following equation:

$$\text{gain} = \frac{x}{0\text{x}400}$$

Note：1) x is controlled by the register 0x0204 & 0x0205.And will be effect when 0x0205 is written.

2) The maximum Analog gain of GC13A0 is 16x.

Table 7-5 detailed registers for analog gain and digital gain control

Address	Register name	Description
0x0204	Gain code	[7:0] Gain code [15:8]
0x0205		[7:0] Gain code [7:0]
0x020e	Digital gain	[5:0] Digital gain [13:8]
0x020f		[7:0] Digital gain [7:0]

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7.7 Binning Mode

Binning read-out can be used to obtain an image of lower resolution for full field of view.

GC13A0 can support 2x2 averaged binning. Pixels of two adjacent rows and columns are averaged before entering the ADC. Figure 7-4 describes the 2x2 averaged binning operation of GC13A0.

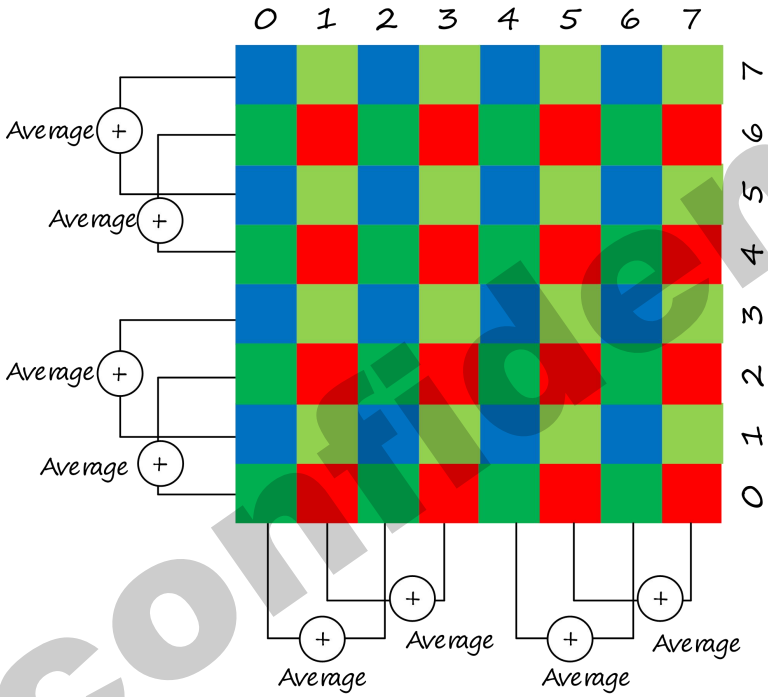

Figure 7-4 Binning Mode

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7.8 Windowing

GC13A0 has a rectangular pixel array 4224 x 3136, it can be windowed by output size control, the output image windowing can be used to adjust output size, and it will affect field angle.

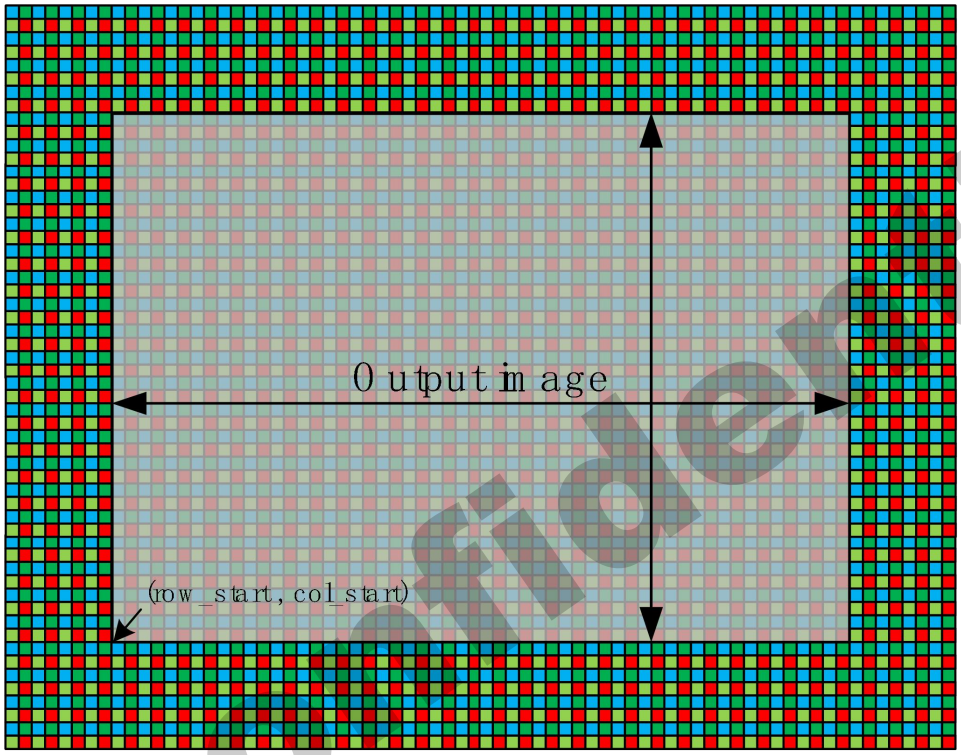

Figure 7-5 Windowing Control

Table 7-6 Detailed Registers for Windowing Control

Address	Register name	Description
0x0351	row_start	[3:0] row_start [11:8]
0x0352		[7:0] row_start [7:0]
0x0353	col_start	[4:0] col_start [12:8]
0x0354		[7:0] col_start [7:0]
0x034c	out_win_width	[4:0] out_win_width[12:8]
0x034d		[7:0] out_win_width[7:0]
0x034e	out_win_height	[3:0] out_win_height[11:8]
0x034f		[7:0] out_ win_height[7:0]

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7.9 Dual Sync Application

GC13A0 supports FSYNC IN/OUT for dual sync master/slave application.

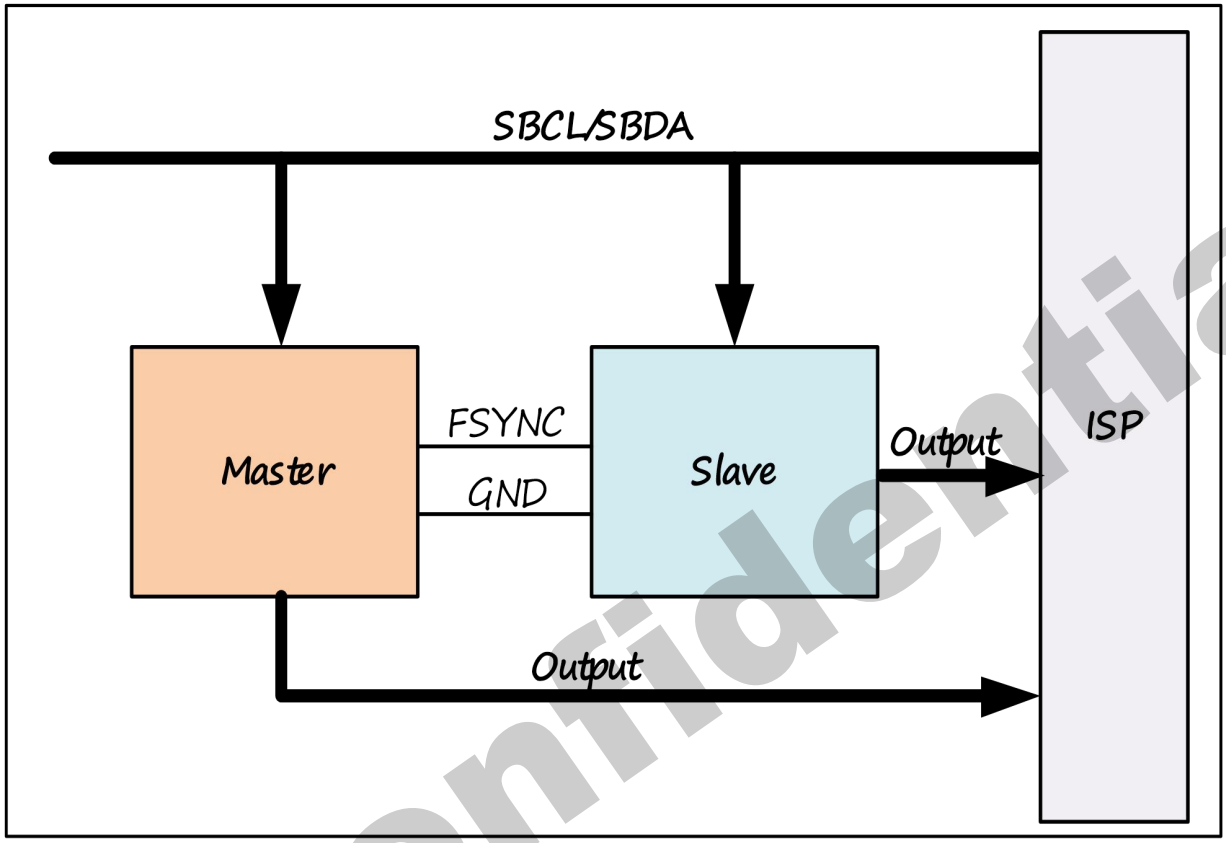

Figure 7-6 Dual Sync Application Configuration

When operating as slave, GC13A0 supports real-time synchronization. After receiving the frame sync signal from master, GC13A0 will firstly clear the row counter to make the frame header align with the master. However, this operation could lead to a corrupted frame so it’s not recommended to start the synchronization operation while streaming.

After the alignment and the image data transmission, the slave will not transmit another frame of image data until it receives next frame sync signal from master, if you want to change frame length while synchronization , it is important to control 2 sensor’s frame length updating with same timing.

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Note:

1. Both the FSYNC pin and GND pin of master and slave should be connected to each other for dual sync application.

2. Frame length should always be set shorter than master when doing AEC in slave mode.

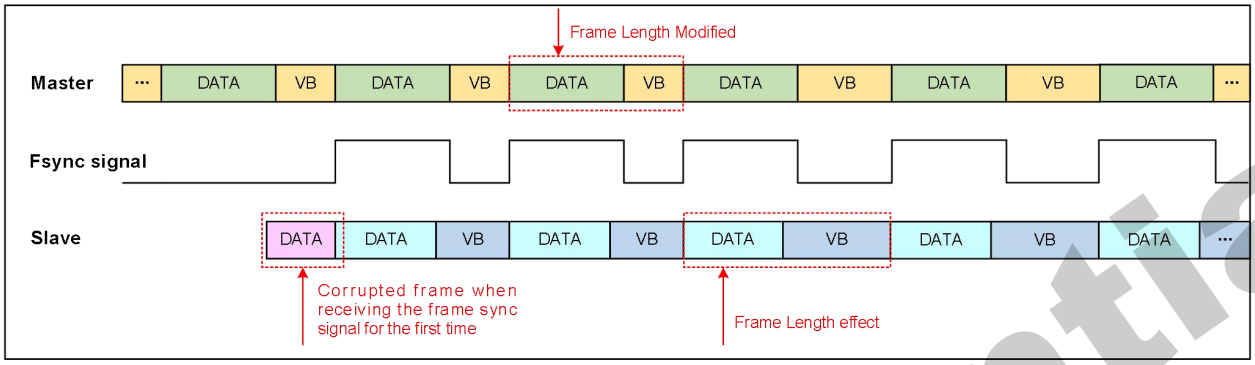

Figure 7-7 Dual Sync Mechanism

Table 7-7 Dual Sync Related Registers

Address	Bit (s)	Register Value		Description
		Master	Slave	
0x02f5	[1]	1	0	Master enable
	[0]	0	1	Slave enable
0x02f0	[4]	1	0	Frame sync out
0x02f6	[7:0]	0x00	0x00	[7:0] position_manual [15:8]
0x02f7	[7:0]	0x08	0x08	[7:0] position_manual [7:0]
0x02e0	[2]	0	1	[2:0] Fsync slave mode
	[1]	0	1	
	[0]	0	1	
0x02df	[3]	1	1	Frame sync clock enable
	[0]	1	1	Frame sync function enable

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7.10 OTP Memory

GC13A0 sensor has 8K bits embedded OTP (One Time Programmable) memory to store manufacturing information and chip identification，also known as fuse ID, and all 8K bits are reserved for Galaxycore. The detailed map arrangement is shown in table 7-8.

Table 7-8 OTP Map Arrangement

Address	Unit(Byte)	Group name	Description
0x0000~0x0010	3	Reserved	Reserved
0x0018	1	Wafer information flag	bit[1:0]: Wafer information flag 00:Empty 01:Valid 1x:Invalid
0x0020~0x0078	12	Fuse ID	Fuse ID
0x0080~0x1ff8	1008	Reserved for GC	Reserved for GC

Normally there are two cases of OTP reading process, one is that the sensor initial setting is loaded before the reading process and the other is that the sensor initial setting is not loaded before the reading process. Figure 7-8 shows the first case while Figure 7-9 shows the second one. The detailed OTP read initial setting as well as the read setting is shown in table 7-9 and table 7-10.

Table 7-9 OTP Read Initial Setting

Read/Write	Address	Value	Description
Write	0x0a67	0x80	[7] otp_en
Write	0x0316	0x01	[0] otpclk_en
Write	0x0313	0x00	init setting
Write	0x0a53	0x04	
Write	0x0a65	0x05	
Write	0x0a68	0x11	
Write	0x0a58	0x00	

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Table 7- 10 OTP Read Setting

Read/Write	Address	Value	Description
Write	0x0a69	0xxx	OTP_addr_H[15:8]
Write	0x0a6a	0xxx	OTP_addr_L[7:0]
Write	0x0313[5]	1	[5] OTP read
Read	0x0a6c	0xxx	OTP read value
	……		

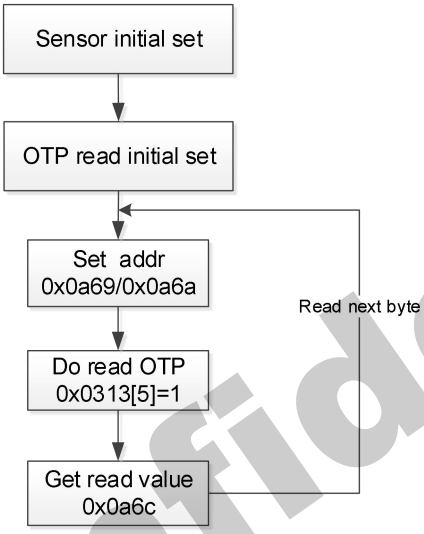

Figure 7- 8 OTP Read Flow with Initial Setting

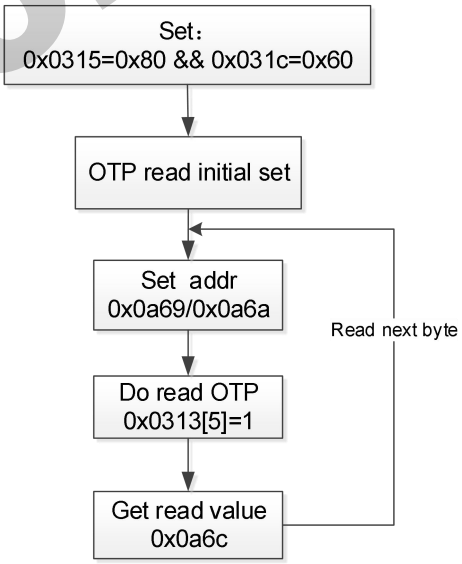

Figure 7- 9 OTP Read Flow without Initial Setting

Note: If you have some question about OTP，please contact our FAE

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7.11 Frame Structure

Frame structure is controlled by HB, frame length, window height, window width and VB.

Frame length control

Frame length is controlled by window height, minimum VB and shutter time.

- Minimum frame length = window height+ min VB + 32 + 16
- If shutter time < minimum frame length-16:

  Actual frame length = minimum frame length
- If shutter time > minimum frame length-16:

  Actual frame length = shutter time + 16 (recommended).

Table 7- 11 Frame Length Control Registers

Address	Register name	Description
0x0340	frame length	[7:0] frame length[15:8]
0x0341		[7:0] frame length[7:0]
0x034a	window height	[3:0] window height [11:8]
0x034b		[7:0] window height [7:0]
0x0226	min vb	[7:0] min vb[15:8]
0x0227		[7:0] min vb[7:0]
0x0202	shutter time	[7:0] shutter time [15:8]
0x0203		[7:0] shutter time [7:0]

Line length control

The Actual Line length is controlled by register 0x0342 & 0x0343, typical actual line length value is 5850 (not recommended to be modified).

Actual Line length = Line length * 3.

Table 7- 12 Frame Structure Related Registers

Address	Register name	Description
0x0342	Line length	[3:0] Line length[11:8]
0x0343		[7:0] Line length[7:0]

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Blank time control

Line blank time is controlled by line length.

Frame blank time is controlled by frame length and out window height,

Frame blank line= frame length– out window height [register(0x034e,0x034f)].

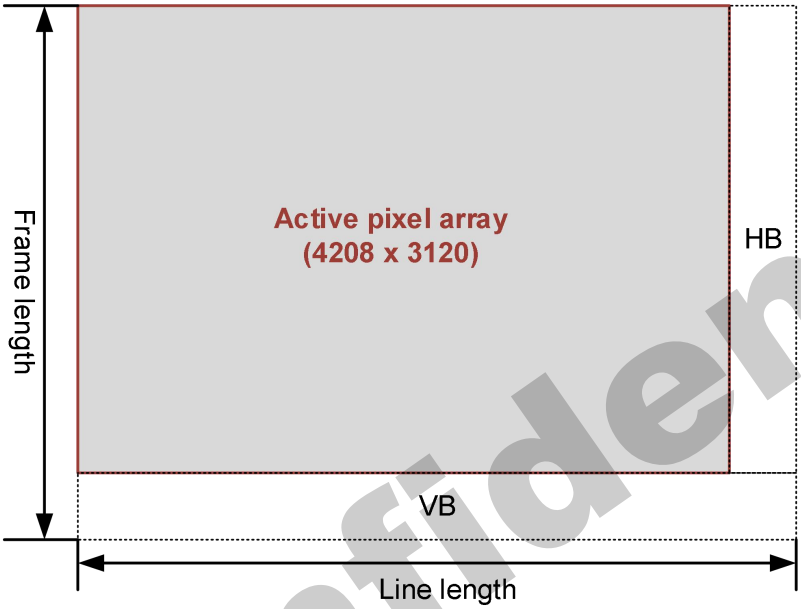

Figure 7- 10 Frame Structure

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7.12 Test Image

GC13A0 supports eight kinds of test image as well as eleven kinds of pure color test image. 0x008d controls the type of test image. The corresponding register value for each kind of test image is shown in the following tables.

Table 7- 13 Register of Test Image

Address	Bits	Name	Description
0x008c	[0]	Test Image en	Enable signal of test image: 1: enable 0: disable

Table 7- 14 Test Image Type

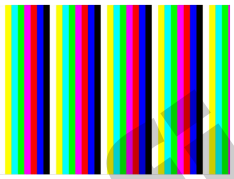
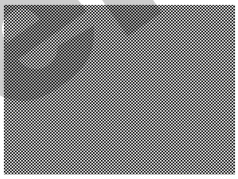
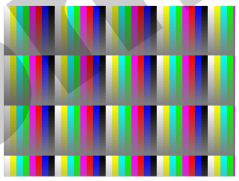
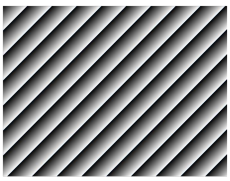
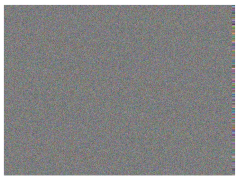
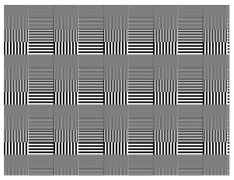
Address	Value	Test Image Type	Value	Test Image Type
0x008d[7:4]	4’h1	 Color bars	4’h5	 Check board
	4’h2	 Fade_to gray Color bars	4’h6	 Slant
	4’h3	 PN9	4’h7	 Resolution
	4’h4	 Horizental gardient		

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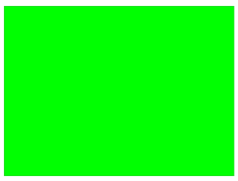
Table 7- 15 Pure Color Image Type

Address	Value	Pure Color Type	Value	Pure Color Type
0x008d[3:0]	4’h0		4’h6	
	4’h1		4’h7	
	4’h2		4’h8	
	4’h3		4’h9	
	4’h4		4’ha	
	4’h5			

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8. Register List

8.1 System Register

Address	Name	Default Value	R/W	Description
0x03f0	**chip_ID_h**	**0x13**	**RO**	**Sensor_ID**
0x03f1	**chip_ID_l**	**0xa0**	**RO**	**Sensor_ID**
0x0c0c	PLLdg_div	0x65	RW	[7:0] plldg_div
0x0336	PLLmp_div	0x7b	RW	[7:0] pllmp_div
0x0202	Shutter time	0x0b	RW	[7:0] shutter time[15:8]
0x0203		0xa0	RW	[7:0] shutter time[7:0]
0x0340	frame_length	0x0b	RW	[7:0] frame_length [15:8]
0x0341		0xa0	RW	[7:0] frame_length [7:0]
0x0342	Line length	0x0b	RW	[5:0] Line length [13:8]
0x0343		0xa0	RW	[7:0] Line length [7:0]
0x0348	win_width	0x10	RW	[4:0]win_width[12:8]
0x0349		0x80	RW	[7:0] win_width[7:0]
0x034a	win_height	0x0c	RW	[3:0] win_height[11:8]
0x034b		0x40	RW	[7:0] win_height[7:0]
0x034c	out_win_width	0x10	RW	[4:0] out_win_width [12:8]
0x034d		0x70	RW	[7:0] out_win_width [7:0]
0x034e	out_win_height	0x0c	RW	[3:0] out_win_height [11:8]
0x034f		0x30	RW	[7:0] out_win_height [7:0]
0x0351	row_start	0x00	RW	[3:0] row_start [11:8]
0x0352		0x08	RW	[7:0] row_start [7:0]
0x0353	col_start	0x00	RW	[4:0] col_start [12:8]
0x0354		0x08	RW	[7:0] col_start [7:0]

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8.2 Gain Control

Address	Name	Default Value	R/W	Description
0x0204	gain code	0x04	RW	[7:0] gain code [15:8]
0x0205		0x00	RW	[7:0] gain code [7:0]
0x020e	Digital gain	0x04	RW	[7:0] Digital gain [15:8]
0x020f		0x00	RW	[7:0] Digital gain [7:0]
0x0090	WB_R_gain	0x04	RW	[3:0] WB_R_gain[11:8]
0x0091		0x00	RW	[7:0] WB_R_gain[7:0]
0x0092	WB_G_gain	0x04	RW	[3:0] WB_G_gain[11:8]
0x0093		0x00	RW	[7:0] WB_G_gain[7:0]
0x0094	WB_B_gain	0x04	RW	[3:0] WB_B_gain[11:8]
0x0095		0x00	RW	[7:0] WB_B_gain[7:0]

8.3 ISP Related

Address	Name	Default Value	R/W	Description
0x0080	block_enable1	0xd0	RW	[4] otp_dd_en
0x0101	Image orientation	0x00	RW	[1] updown [0] mirror
0x008c	test image enable	0x00	RW	[0] out test image
0x008d	test image mode	0x10	RW	[7:4] test image mode [3:0] solid_color_value
0x009b	WB_offset	0x40	RW	[7:0] WB_offset
0x00a0	PDAF DD	0x11	RW	[5] PD DD en

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8.4 OTP

Address	Name	Default Value	R/W	Description
0x0313	OTP	0x00	RW	[7] reserved [6] OTP_write (WO) [5] OTP_read (WO) [4:0] reserved
0x0316	PLL_mode1	0x00	RW	[3] otpclk_en
0x0a67	OTP_mode	0x00	RW	[7] OTP_en
0x0a69	OTP_access_addr	0x00	RW	[7:0] OTP_addr[15:8]
0x0a6a		0x00	RW	[7:0] OTP_addr[7:0]
0x0a6b	OTP_write_value	0x00	RW	[7:0] OTP_write_value
0x0a6c	OTP_read_value		RO	[7:0] OTP_read_value

8.5 Embedded Data Line

Address	Name	Default Value	R/W	Description
0x03a0	EMBEDL_en	0x00	RW	[1] EMBEDL_clk_en [0] EMBEDL_en
0x01ca	EMBEDL_FLAG		RO	[3] EMBEDL_lasts [2] EMBEDL_finish [1] first_illegal [0] EMBEDL_legal

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8.6 MIPI

Address	Name	Default Value	R/W	Description
0x0100	standby	0x00	RW	[0] standby 0:sw_standby 1:streaming
0x0102	MIPI	0x00	RW	[3] Lane_En [0] MIPI_En
0x0114	mipi_lane_num	0x03	RW	[1:0] mipi_lane_num
0x0115	DPHY_mode	0x10	RW	[1:0] clk lane mode
0x0116	LP_set	0x29	RW	[7:6] LP_Z [5:4] LP_NEW [3:2] LP_ONE [1:0] LP_ZERO
0x0120	T_init_set	0x80	RW	T_init_set
0x0121	T_LPX_set	0x12	RW	T_LPX_set
0x0122	T_CLK_HS_PREPARE_set	0x0d	RW	T_CLK_HS_PREPARE_set
0x0123	T_CLK_zero_set	0x4b	RW	T_CLK_zero_set
0x0124	T_CLK_PRE_set	0x02	RW	T_CLK_PRE_set
0x0125	T_CLK_POST_set	0x16	RW	T_CLK_POST_set
0x0126	T_CLK_TRAIL_set	0x0f	RW	T_CLK_TRAIL_set
0x0127	T_HS_exit_set	0x10	RW	T_HS_exit_set
0x0128	T_wakeup_set	0x0f	RW	T_wakeup_set
0x0129	T_HS_PREPARE_set	0x0d	RW	T_HS_PREPARE_set
0x012a	T_HS_Zero_set	0x1f	RW	T_HS_Zero_set
0x012b	T_HS_TRAIL_set	0x10	RW	T_HS_TRAIL_set

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0x0180	DPHY_mode1	0x06	RW	[3:0] dphy_mipi_diff
0x0182	DPHY_mode3	0x55	RW	[7:6] data3ctr [5:4] data2ctr [3:2] data1ctr [1:0] data0ctr

8.7 Dual Sync

Address	Name	Default Value	R/W	Description
0x02f0	fsync_pad_mode	0x00	RW	[4] vsync_out_mode [3] fsync_out_polarity [2:0] reserved
0x02f5	fsync_every_mode	0xb0	RW	[4] fsync_every_clr_fcnt_mode [3:2] reserved [1] fsync_every_frame_master [0] fsync_every_frame_slave
0x02f6	position_manual	0x00	RW	[7:0] position_manual[15:8]
0x02f7		0x02	RW	[7:0] position_manual[7:0]
0x02e0	fsync_rc_mode	0x20	RW	[7:3] reserved [2] fine_Rowcnt _mode1 [1] fine_Rowcnt _mode2 [0] RowCnt mode en
0x02df	fsync_mode	0x08	RW	[7:4]reserved [3] fsync_clock_en [2:1] reserved [0] fsync_en

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